

Features

- 100V/80A,
 $R_{DS(ON)} = 15m\Omega(Typ.)@V_{GS}=10V$
 $R_{DS(ON)} = 17m\Omega(Typ.)@V_{GS}=4.5V$
- Planar Technology
- High Ruggedness
- Enhanced FBSOA for superior linear mode operation
- 100% Avalanche Tested

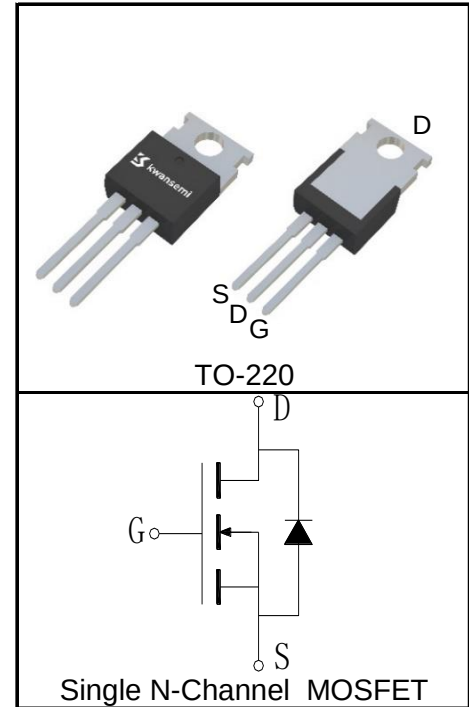
Applications

- Motor Control
- Power Management in Inverter System



Halogen-Free

Pin Description



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
Common Ratings ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)			
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	
T_{Jmax}	Maximum Junction Temperature	175	$^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$ 80	A
Mounted on Large Heat Sink			
$I_{DP}^{①}$	Pulse Drain Current	$T_C=25^\circ\text{C}$ 320	A
$I_D^{②}$	Continuous Drain Current($V_{GS}=10V$)	$T_C=25^\circ\text{C}$ 80	A
		$T_C=100^\circ\text{C}$ 56	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$ 340	W
		$T_C=100^\circ\text{C}$ 170	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	0.44	$^\circ\text{C/W}$
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	62.5	$^\circ\text{C/W}$
Drain-Source Avalanche Ratings			
$E_{AS}^{④}$	Avalanche Energy, Single Pulsed	1156	mJ

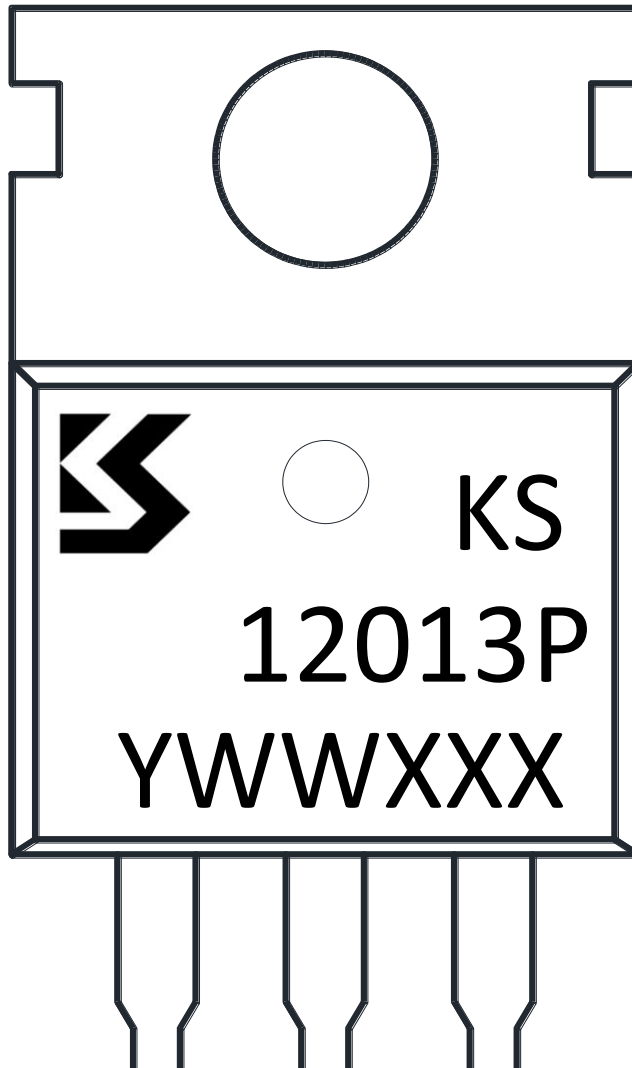
Electrical Characteristics ($T_C=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	KS12013CAP			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V			1	μA
		T _J =125°C			30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1.1	1.4	2.3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
R _{DS(ON)} ^⑤	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =40A		15	20	mΩ
		V _{GS} =4.5V, I _{DS} =20A		17	23	mΩ
Diode Characteristics						
V _{SD} ^⑤	Diode Forward Voltage	I _{SD} =40A, V _{GS} =0V		0.84	1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} =40A, dI _{SD} /dt=100A/μs		64		ns
Q _{rr}	Reverse Recovery Charge			205		nC
Dynamic Characteristics ^⑥						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz		1.3		Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, Frequency=1.0MHz		2800		pF
C _{oss}	Output Capacitance			385		
C _{rss}	Reverse Transfer Capacitance			145		
t _{d(ON)}	Turn-on Delay Time	V _{DD} =50V, I _{DS} =40A, V _{GEN} =10V, R _G =6Ω		23		ns
t _r	Turn-on Rise Time			35		
t _{d(OFF)}	Turn-off Delay Time			71		
t _f	Turn-off Fall Time			20		
Gate Charge Characteristics ^⑥						
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V, I _{DS} =40A		150		nC
Q _{gs}	Gate-Source Charge			7.3		
Q _{gd}	Gate-Drain Charge			51		

- Notes:
- ① Pulse width limited by safe operating area.
 - ② Calculated continuous current based on maximum allowable junction temperature. The package limitation current is 75A.
 - ③ When mounted on 1 inch square copper board, $t \leq 10\text{sec}$. The value in any given application depends on the user's specific board design.
 - ④ Limited by T_{Jmax} , Starting $T_J = 25^{\circ}\text{C}$, $I_{ASmax} = 68A$, $L = 0.5\text{mH}$, $V_{DD} = 50V$, $R_G = 25\Omega$, $V_{GS} = 10V$. Part not recommended for use above this value. 100% Final Test at $I_{AS} = 48A$, $L = 0.5\text{mH}$.
 - ⑤ Pulse test; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 - ⑥ Guaranteed by design, not subject to production testing.

Ordering and Marking Information

Device	Package	Packaging	Quantity	Reel Size	Tape width
KS12013CAP	TO-220	Tube	50	-	-

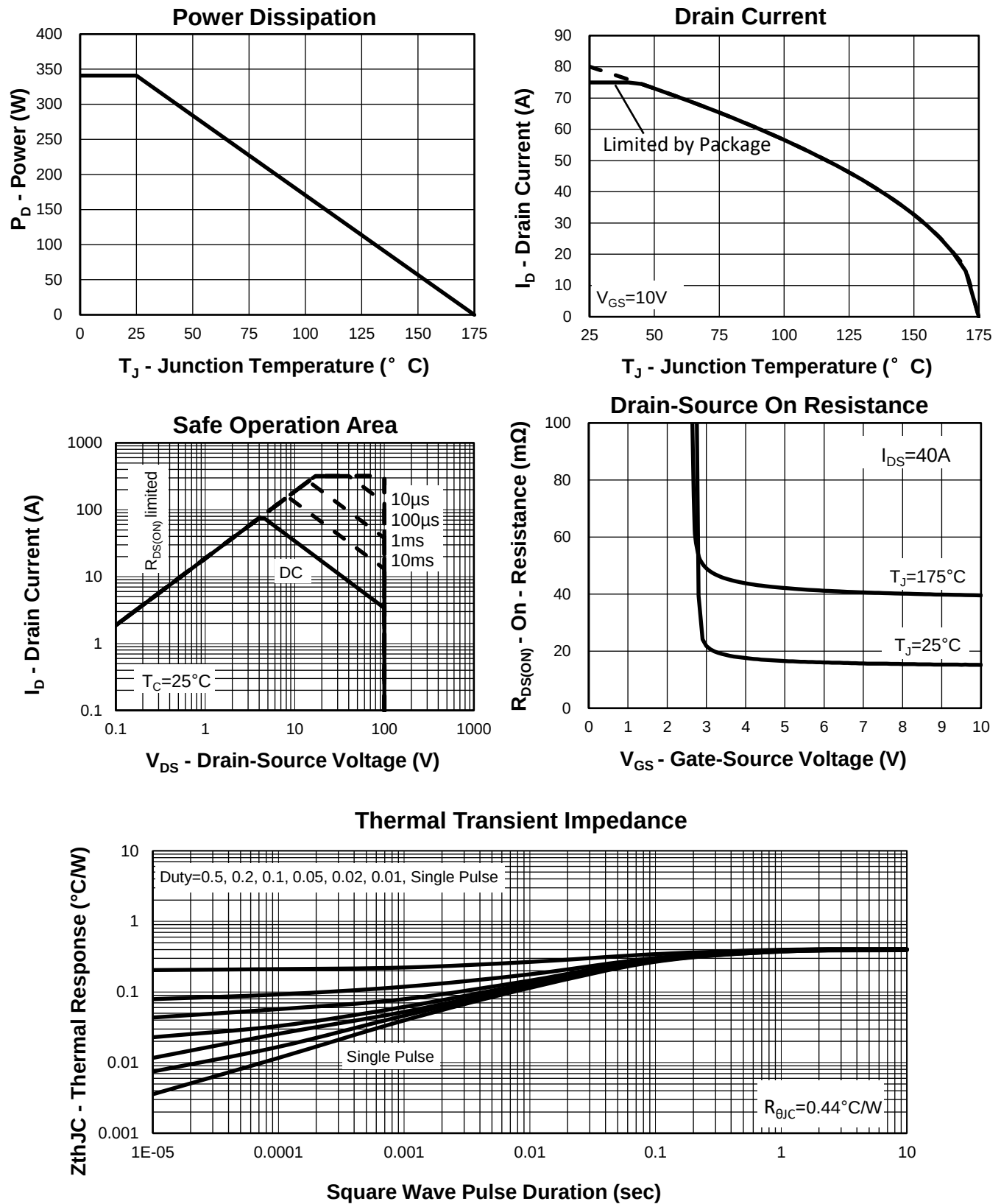


1st Line: Kwansemi LOGO, Kwansemi Code(KS)

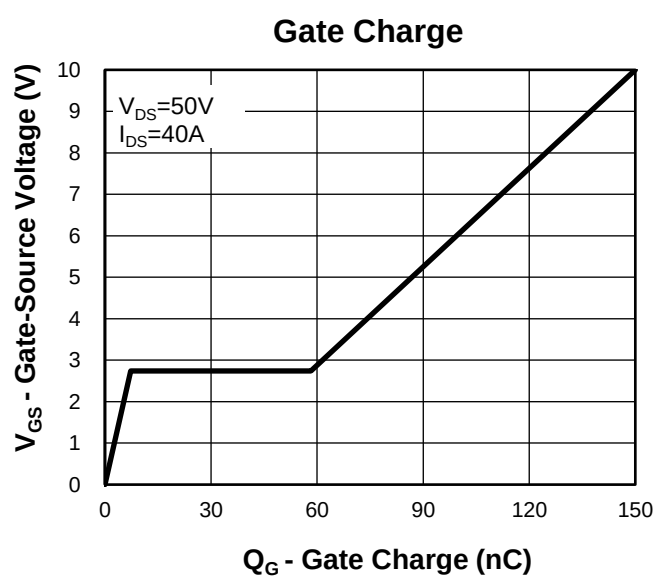
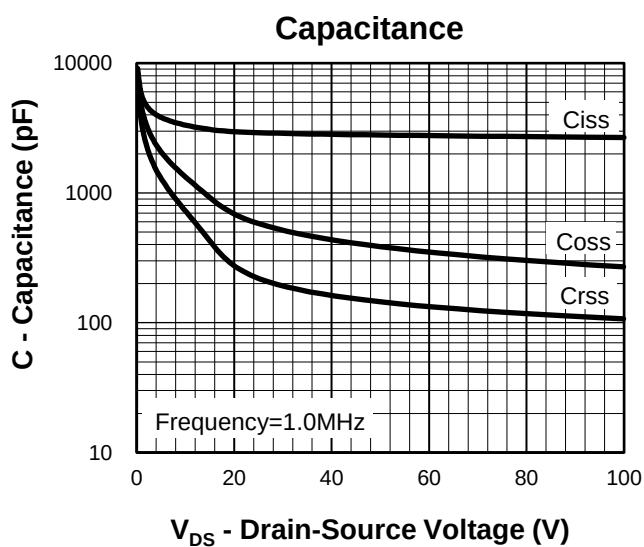
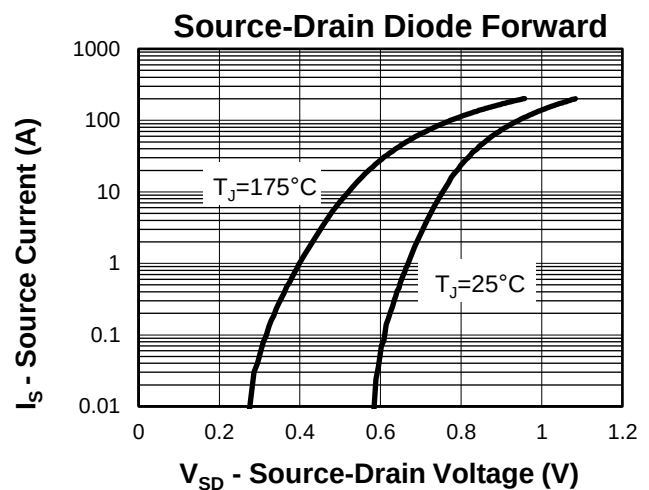
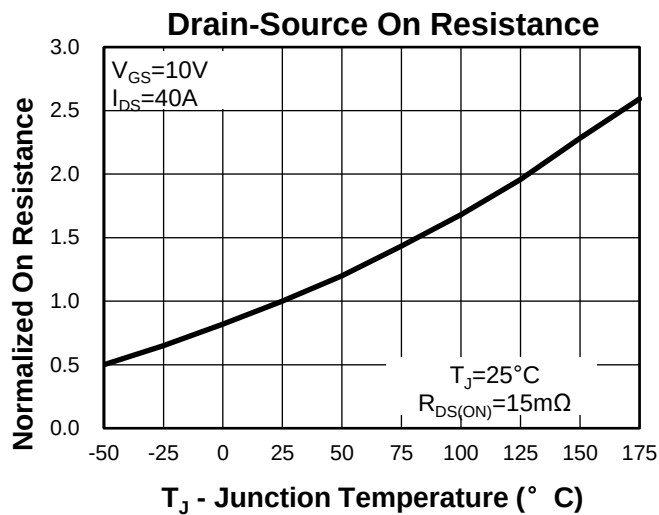
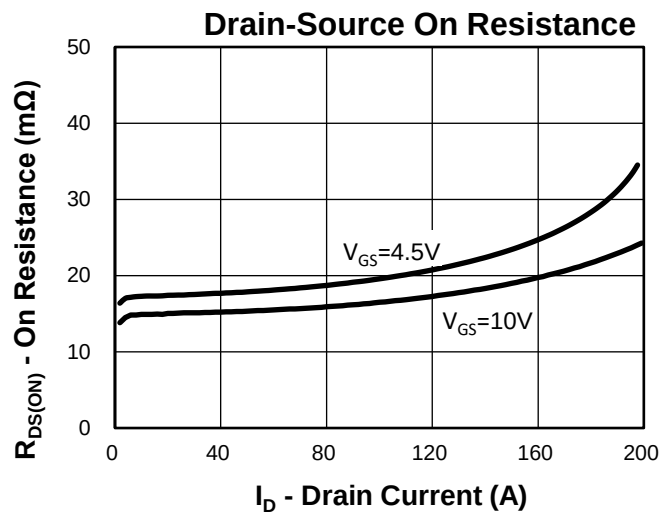
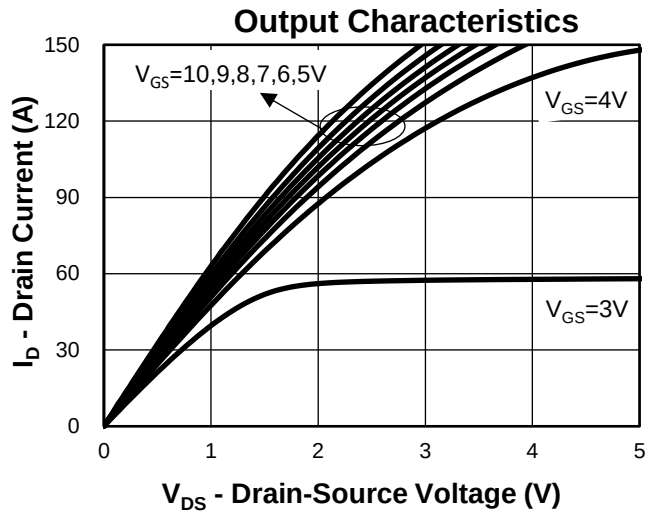
2nd Line: Part Number(12013P)

3rd Line: Lot Number(YWWXXX)

Typical Characteristics

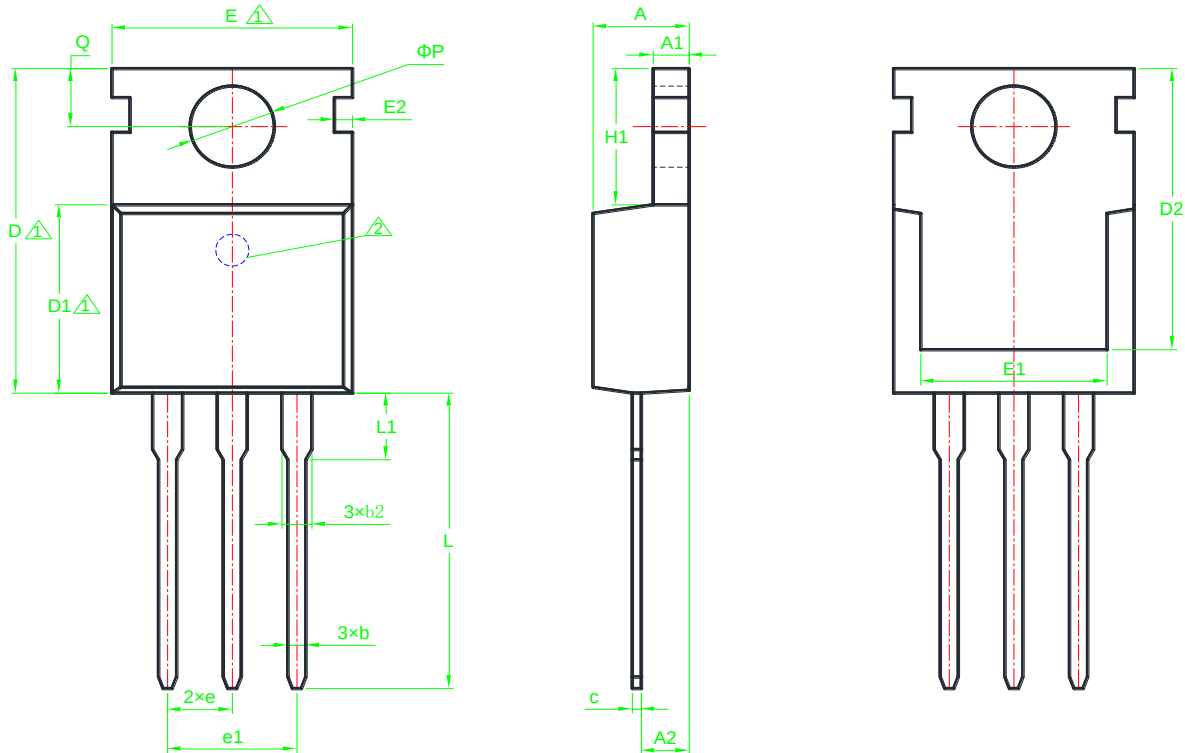


Typical Characteristics



Package Information

TO-220

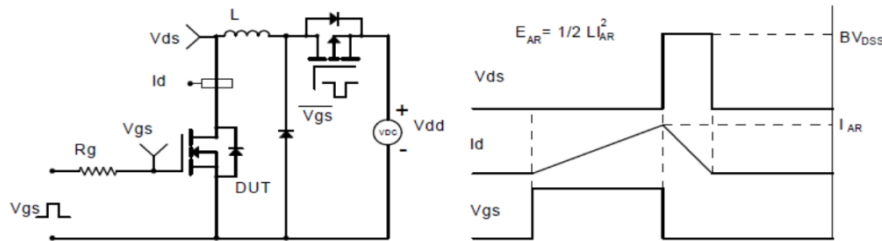


SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.55	4.80	0.169	0.179	0.189	E1	7.00	*	8.40	0.276	*	0.331
A1	1.20	1.30	1.45	0.047	0.051	0.057	E2	*	*	0.75	*	*	0.030
A2	2.20	2.40	2.70	0.087	0.094	0.106	e	2.54BSC			0.100BSC		
b	0.70	0.80	0.95	0.028	0.031	0.037	e1	5.08BSC			0.200BSC		
b2	1.15	1.35	1.50	0.045	0.053	0.059	H1	6.30	6.50	6.80	0.248	0.256	0.268
c	0.40	0.50	0.60	0.016	0.020	0.024	L	12.70	13.20	13.90	0.500	0.520	0.547
D	15.10	15.60	16.10	0.594	0.614	0.634	L1	2.85	*	3.50	0.112	*	0.138
D1	8.75	9.20	9.65	0.344	0.362	0.380	ØP	3.50	3.65	3.80	0.138	0.144	0.150
D2	12.20	12.50	12.80	0.480	0.492	0.504	Q	2.70	*	2.90	0.106	*	0.114
E	9.70	10.00	10.30	0.382	0.394	0.406							

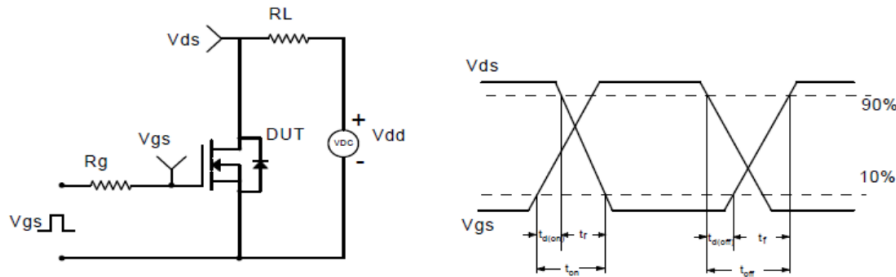
① Dimensions D and D1 and E do not include mold flash protrusions or gate burrs.

② The existence and size of demolding hole are variable depending on mold.

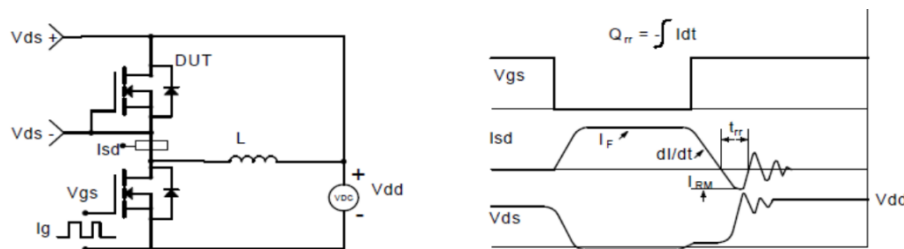
Avalanche Test Circuit and Waveforms



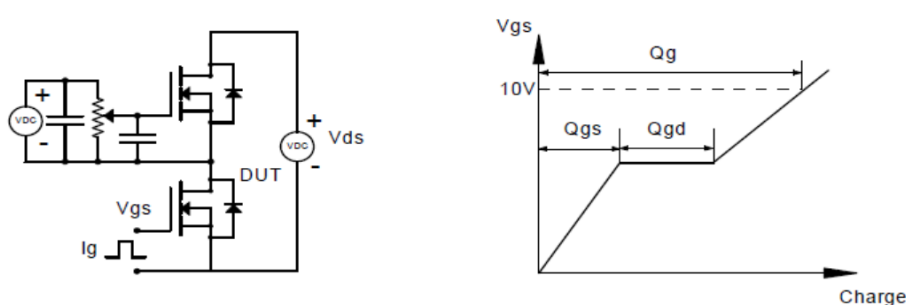
Switching Time Test Circuit and Waveforms



Diode Recovery Test Circuit and Waveforms



Gate Charge Test Circuit and Waveform



Customer Service

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