

Features

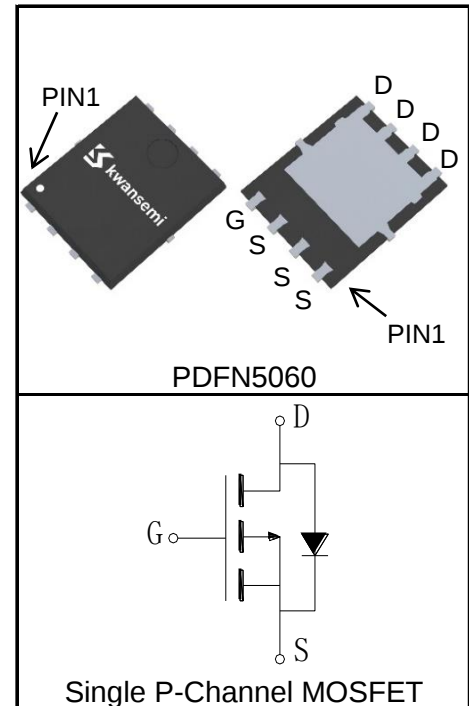
- -30V/-79A,
 $R_{DS(ON)} = 4.3m\Omega(Typ.)@V_{GS}=-10V$
 $R_{DS(ON)} = 6.2m\Omega(Typ.)@V_{GS}=-4.5V$
- Low $R_{DS(ON)}$
- Super High Dense Cell Design
- Fast Switching Speed
- 100% avalanche tested
- 100% Rg Tested

Applications

- Switching Application Systems



Pin Description



Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
Common Ratings (T _C =25°C Unless Otherwise Noted)				
V _{DSS}	Drain-Source Voltage		-30	V
V _{GSS}	Gate-Source Voltage		±20	
T _{Jmax}	Maximum Junction Temperature		150	°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to 150	°C
I _S	Diode Continuous Forward Current	T _C =25°C	-79	A
Mounted on Large Heat Sink				
I _{DP} ^①	Pulse Drain Current	T _C =25°C	-316	A
I _D ^②	Continuous Drain Current@T _C (V _{GS} =-10V)	T _C =25°C	-79	A
		T _C =100°C	-50	
	Continuous Drain Current@T _A (V _{GS} =-10V) ^③	T _A =25°C	-22	
		T _A =70°C	-18	
P _D	Maximum Power Dissipation@T _C	T _C =25°C	50	W
		T _C =100°C	20	
	Maximum Power Dissipation@T _A ^③	T _A =25°C	4.2	
		T _A =70°C	2.7	

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.5	°C/W
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	30	°C/W
Drain-Source Avalanche Ratings			
$E_{AS}^{④}$	Avalanche Energy, Single Pulsed	324	mJ

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	KS3305NA			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250μA	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
			T _J =125°C			
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250μA	-1.1	-1.6	-2.3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
R _{DS(ON)} ⑤	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-20A		4.3	5.5	mΩ
		V _{GS} =-4.5V, I _{DS} =-15A		6.2	8	mΩ
Diode Characteristics						
V _{SD} ⑤	Diode Forward Voltage	I _{SD} =-20A, V _{GS} =0V		-0.83	-1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} =-20A, dI _{SD} /dt=100A/μs		32		ns
Q _{rr}	Reverse Recovery Charge			60		nC
Dynamic Characteristics ⑥						
R _G	Gate Resistance	V _{GS} =0V,V _{DS} =0V,F=1MHz		15		Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, Frequency=1.0MHz		3820		pF
C _{oss}	Output Capacitance			625		
C _{rss}	Reverse Transfer Capacitance			410		
t _{d(ON)}	Turn-on Delay Time	V _{DD} =-15V, I _{DS} =-20A, V _{GS} =-10V,R _G =3Ω		33		ns
t _r	Turn-on Rise Time			85		
t _{d(OFF)}	Turn-off Delay Time			121		
t _f	Turn-off Fall Time			46		
Gate Charge Characteristics ⑥						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _{DS} =-20A		69		nC
Q _{gs}	Gate-Source Charge			12		
Q _{gd}	Gate-Drain Charge			16		

Notes:

- ①Pulse width limited by safe operating area.
- ②Calculated continuous current based on maximum allowable junction temperature. The package limitation current is 50A.
- ③When mounted on 1 inch square copper board, $t \leq 10\text{sec}$.
- ④Limited by $T_{j\text{max}}$, Starting $T_j = 25^\circ\text{C}$, $I_{AS\text{max}} = -36\text{A}$, $L=0.5\text{mH}$, $V_{DD} = -20\text{V}$, $R_G = 25\Omega$, $V_{GS} = -10\text{V}$. Part not recommended for use above this value. 100% Final Test at $I_{AS} = -20\text{A}$, $L=0.5\text{mH}$.
- ⑤Pulse test; Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- ⑥Guaranteed by design, not subject to production testing.

Ordering and Marking Information

Device	Package	Packaging	Quantity	Reel Size	Tape width
KS3305NA	PDFN5060	Tape&Reel	5000	13"	12mm

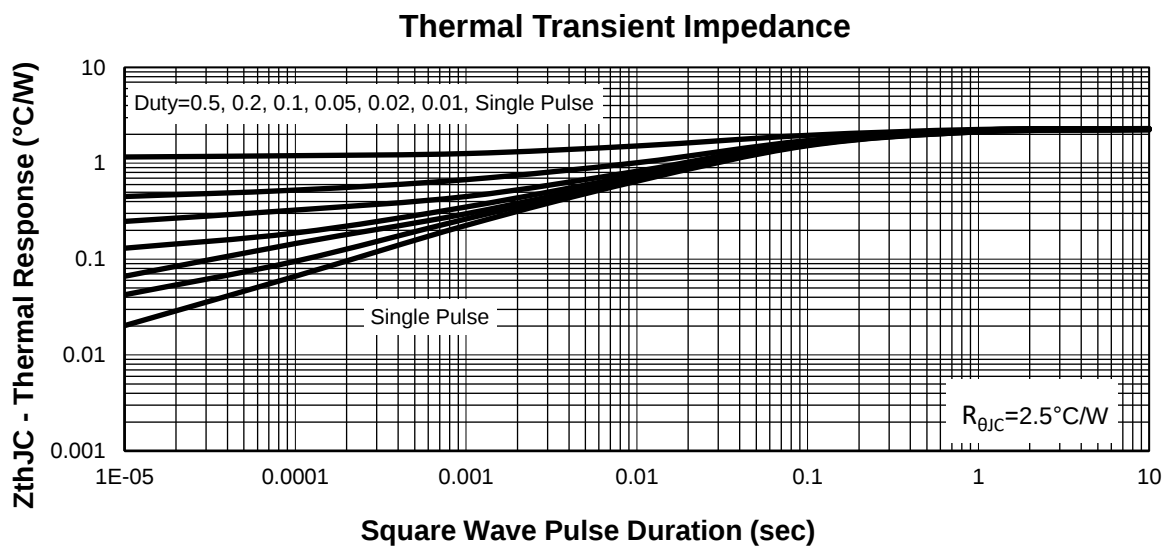
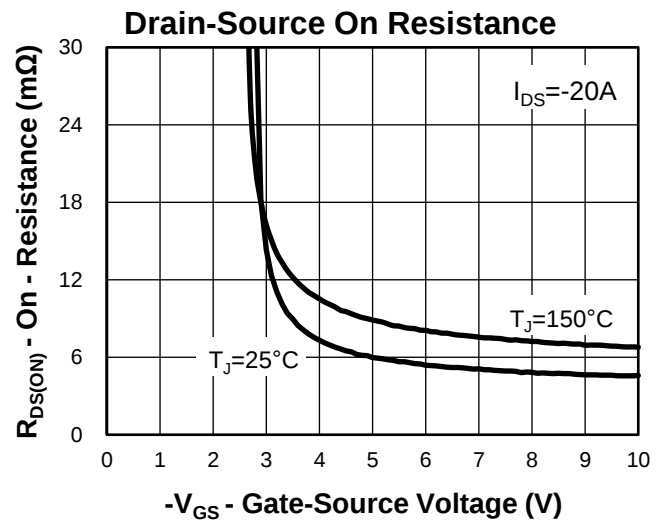
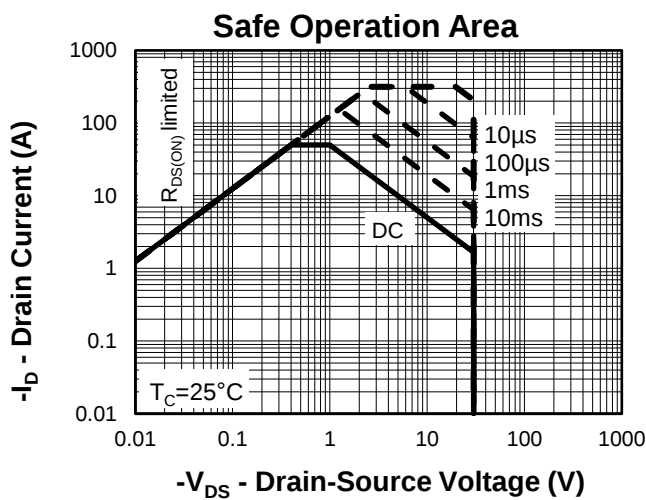
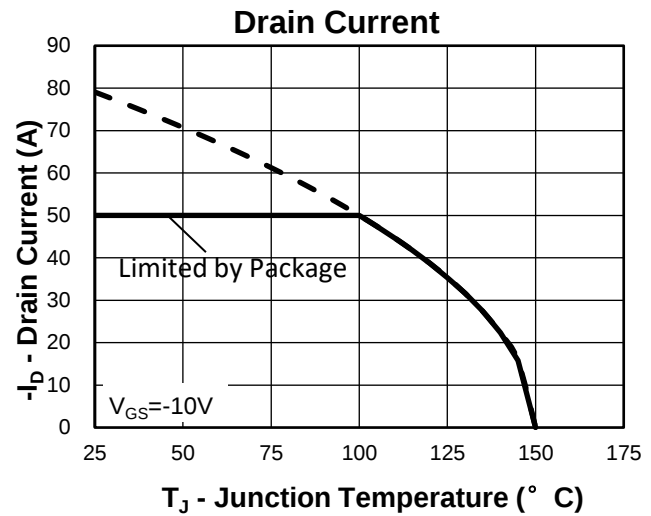
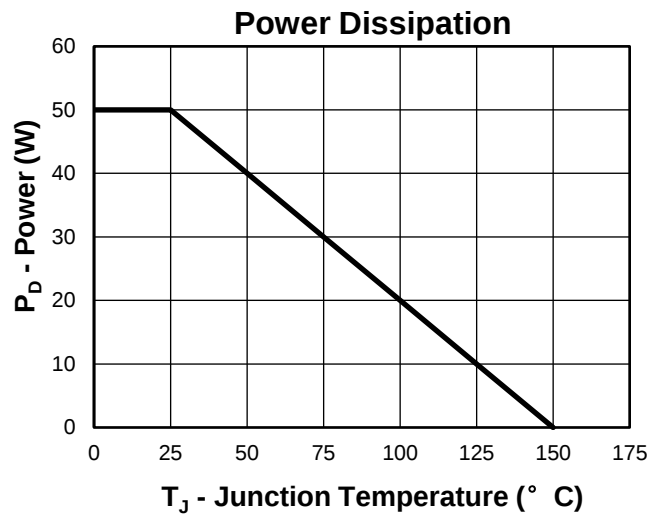


1st Line: Kwansemi LOGO, Kwansemi Code(KS)

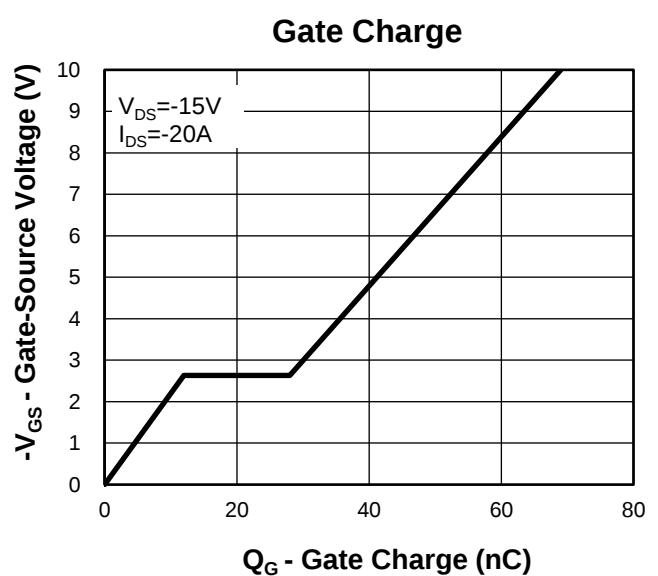
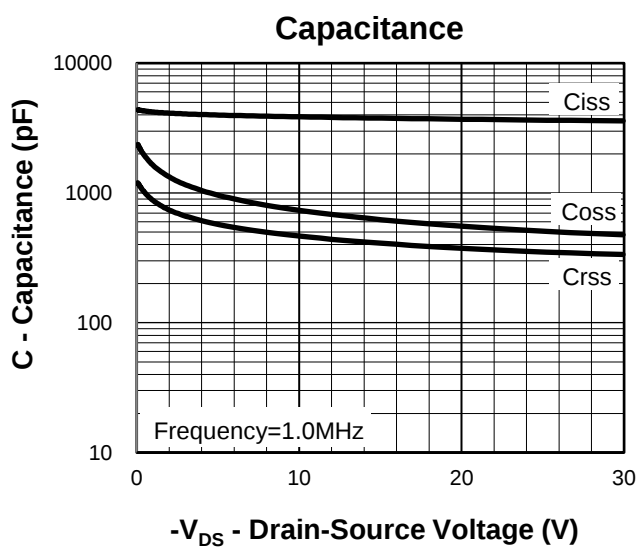
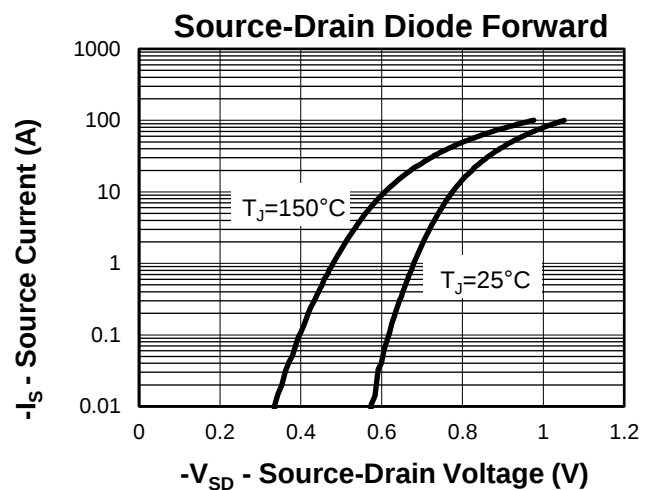
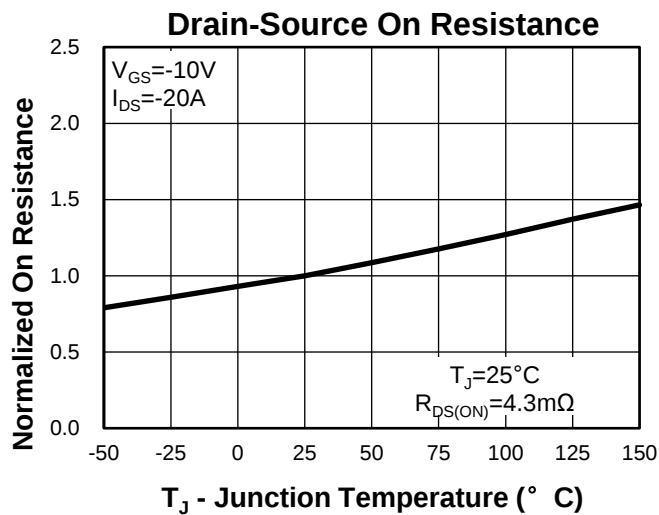
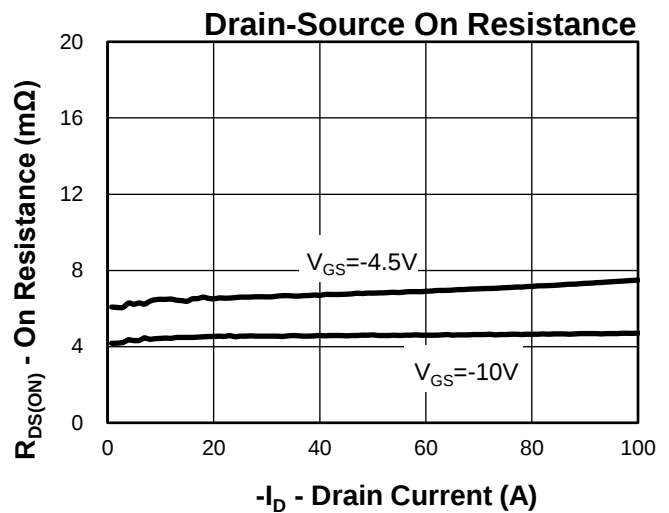
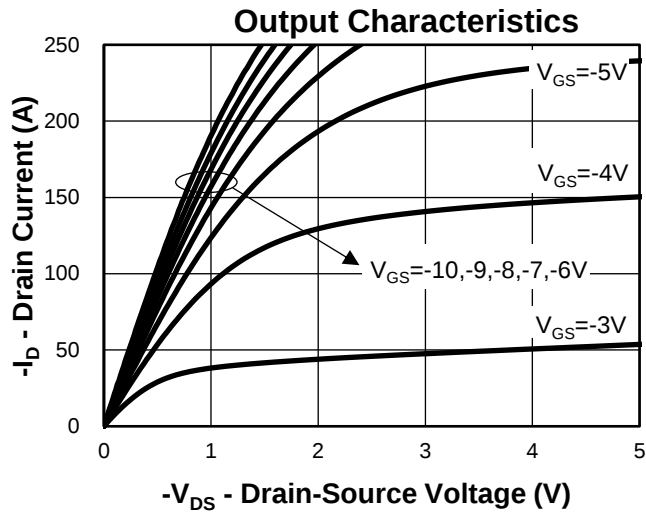
2nd Line: Part Number(3305)

3rd Line: Lot Number(YWWXXX)

Typical Characteristics

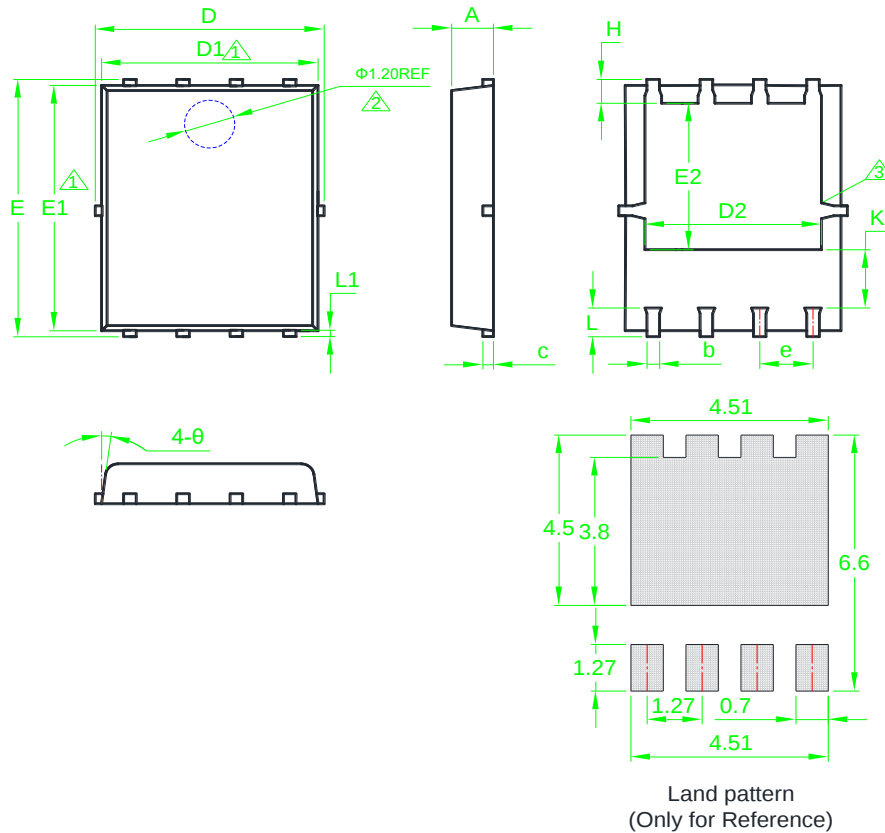


Typical Characteristics



Package Information

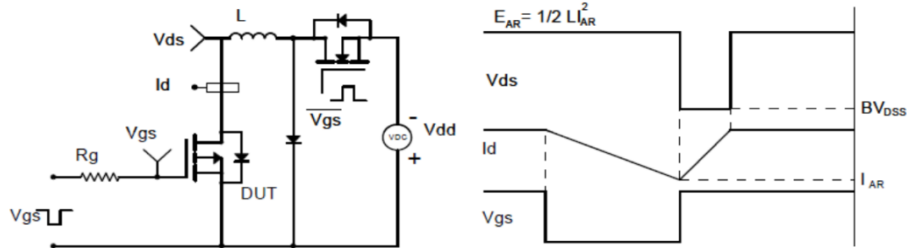
PDFN5060



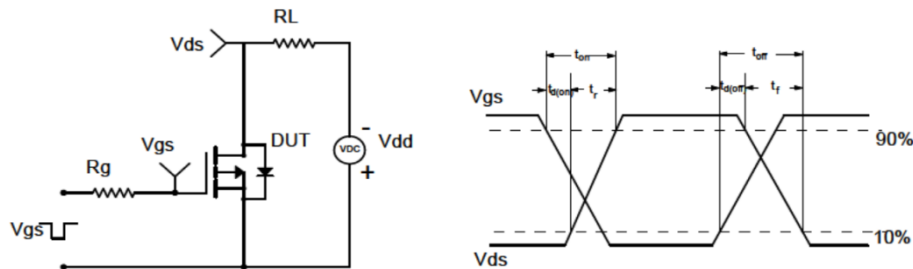
SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.20	0.035	0.039	0.047	E2	3.27	3.50	3.90	0.129	0.138	0.154
b	0.25	*	0.50	0.010	*	0.020	e	1.27BSC			0.050BSC		
c	0.20	0.25	0.30	0.008	0.010	0.012	H	0.41	0.51	0.71	0.016	0.020	0.028
D	5.15BSC			0.203BSC			K	1.10	1.35	1.50	0.043	0.053	0.059
D1	4.80	5.00	5.40	0.189	0.197	0.213	L	0.51	0.61	0.71	0.020	0.024	0.028
D2	3.60	*	4.40	0.142	*	0.173	L1	0.06	0.13	0.30	0.002	0.005	0.012
E	5.90	6.15	6.30	0.232	0.242	0.248	θ	0°	*	12°	0°	*	12°
E1	5.40	5.80	5.95	0.213	0.228	0.234							

- △1 Dimensions D1 and E1 do not include mold flash protrusions or gate burrs.
- △2 The existence and size of demolding hole are variable depending on mold.
- △3 The size and shape of exposed pad are variable depending on mold.

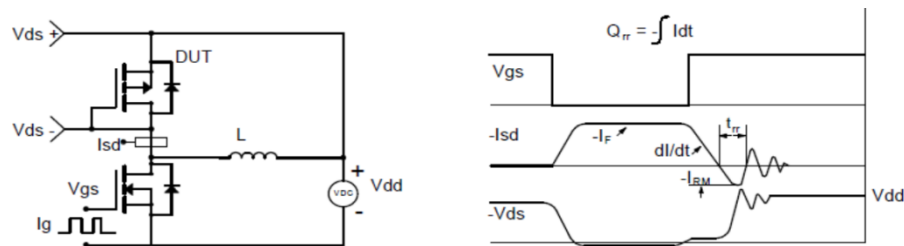
Avalanche Test Circuit and Waveforms



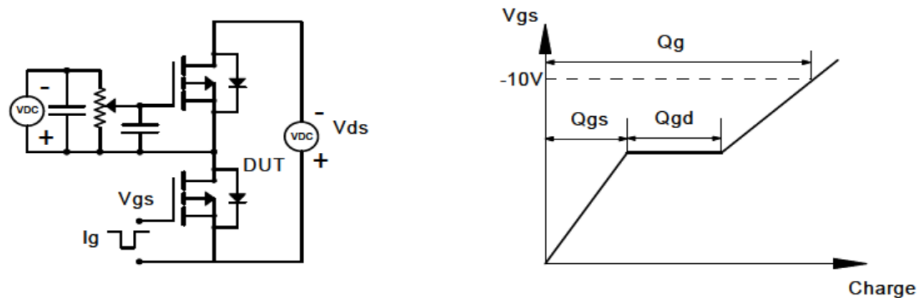
Switching Time Test Circuit and Waveforms



Diode Recovery Test Circuit and Waveforms



Gate Charge Test Circuit and Waveform



Customer Service

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