

Features

- 68V80A,
 $R_{DS(ON)} = 7m\Omega(Typ.)@V_{GS}=10V$
- Low $R_{DS(ON)}$
- Super High Dense Cell Design
- Low Gate Charge
- 100% Avalanche Tested

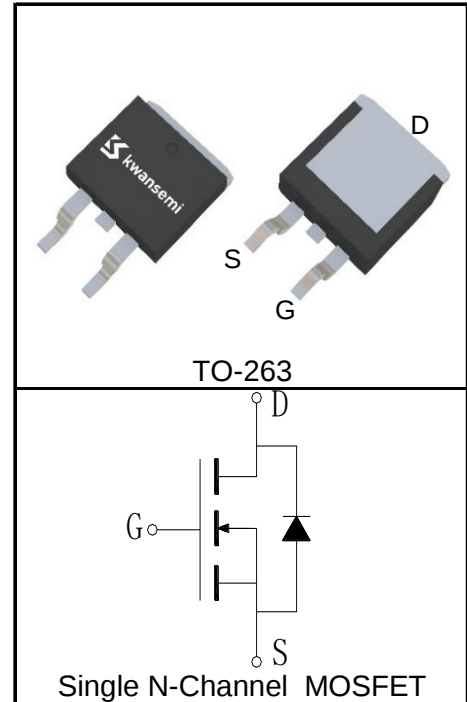
Applications

- DC-DC Converters
- Power Supply



Halogen-Free

Pin Description



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
Common Ratings ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)			
V_{DSS}	Drain-Source Voltage	68	V
V_{GSS}	Gate-Source Voltage	± 25	V
T_{Jmax}	Maximum Junction Temperature	175	$^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$ 80	A
Mounted on Large Heat Sink			
$I_{DP}^{①}$	Pulse Drain Current	$T_C=25^\circ\text{C}$ 320	A
$I_D^{②}$	Continuous Drain Current($V_{GS}=10V$)	$T_C=25^\circ\text{C}$ 80	A
		$T_C=100^\circ\text{C}$ 63	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$ 115	W
		$T_C=100^\circ\text{C}$ 57	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.3	$^\circ\text{C/W}$
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	62.5	$^\circ\text{C/W}$
Drain-Source Avalanche Ratings			
$E_{AS}^{④}$	Avalanche Energy, Single Pulsed	342	mJ

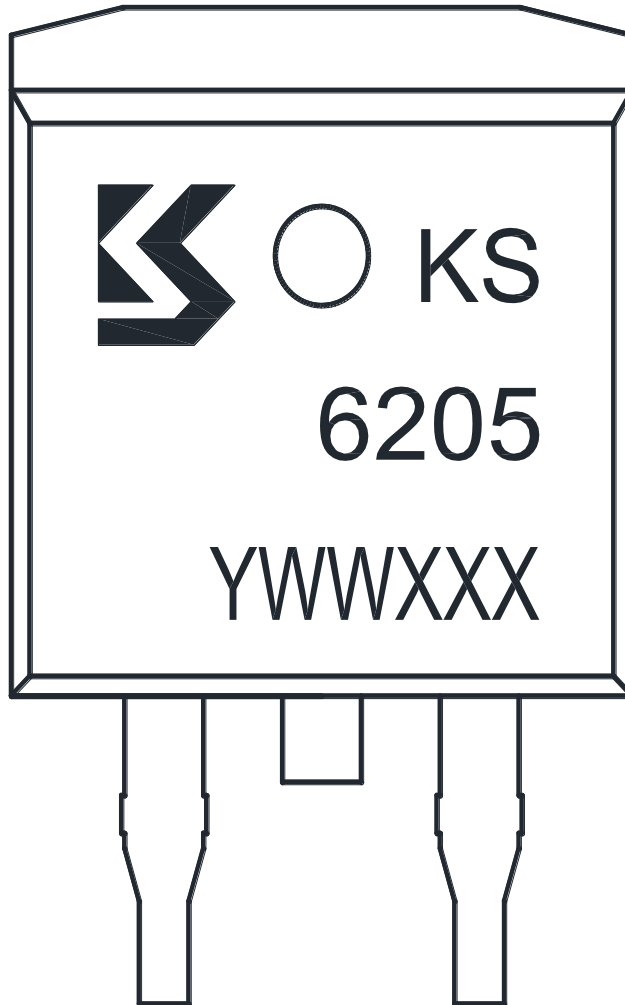
Electrical Characteristics ($T_C=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	KS6205GA			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	68			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =68V, V _{GS} =0V			1	μA
		T _J =125°C			30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	2	3	4	V
I _{GSS}	Gate Leakage Current	V _{GS} =±25V, V _{DS} =0V			±100	nA
R _{DS(ON)} ⑤	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =40A		7	8.5	mΩ
		V _{GS} =6V, I _{DS} =20A		9.5	13	mΩ
Diode Characteristics						
V _{SD} ⑤	Diode Forward Voltage	I _{SD} =40A, V _{GS} =0V		0.84	1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} =40A, dI _{SD} /dt=100A/μs		25		ns
Q _{rr}	Reverse Recovery Charge			37		nC
Dynamic Characteristics ⑥						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz		0.9		Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, Frequency=1MHz		3875		pF
C _{oss}	Output Capacitance			220		
C _{rss}	Reverse Transfer Capacitance			210		
t _{d(ON)}	Turn-on Delay Time	V _{DD} =30V, I _{DS} =40A, V _{GEN} =10V, R _G =3Ω		18		ns
t _r	Turn-on Rise Time			27		
t _{d(OFF)}	Turn-off Delay Time			54		
t _f	Turn-off Fall Time			26		
Gate Charge Characteristics ⑥						
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _{DS} =40A		79		nC
Q _{gs}	Gate-Source Charge			18		
Q _{gd}	Gate-Drain Charge			26		

- Notes:
- ① Pulse width limited by safe operating area.
 - ② Calculated continuous current based on maximum allowable junction temperature. The package limitation current is 75A.
 - ③ When mounted on 1 inch square copper board, $t \leq 10\text{sec}$. The value in any given application depends on the user's specific board design.
 - ④ Limited by T_{Jmax} , Starting $T_J = 25^{\circ}\text{C}$, $I_{ASmax} = 37A$, $L = 0.5\text{mH}$, $V_{DD} = 32V$, $R_G = 25\Omega$, $V_{GS} = 10V$. Part not recommended for use above this value. 100% Final Test at $I_{AS} = 25A$, $L = 0.5\text{mH}$.
 - ⑤ Pulse test; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 - ⑥ Guaranteed by design, not subject to production testing.

Ordering and Marking Information

Device	Package	Packaging	Quantity	Reel Size	Tape width
KS6205GA	TO-263	Tape&Reel	800	13"	24mm

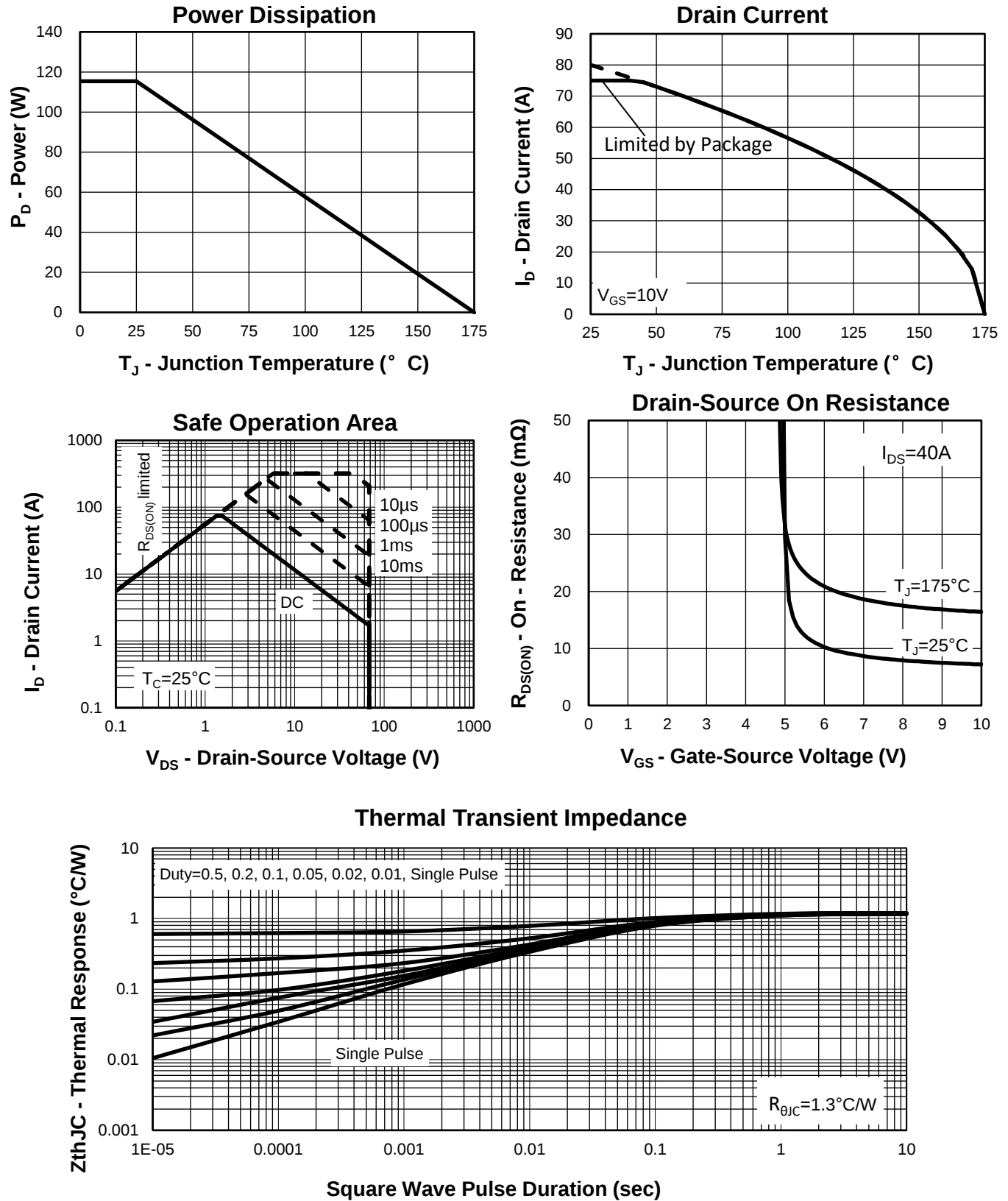


1st Line: Kwansemi LOGO, Kwansemi Code(KS)

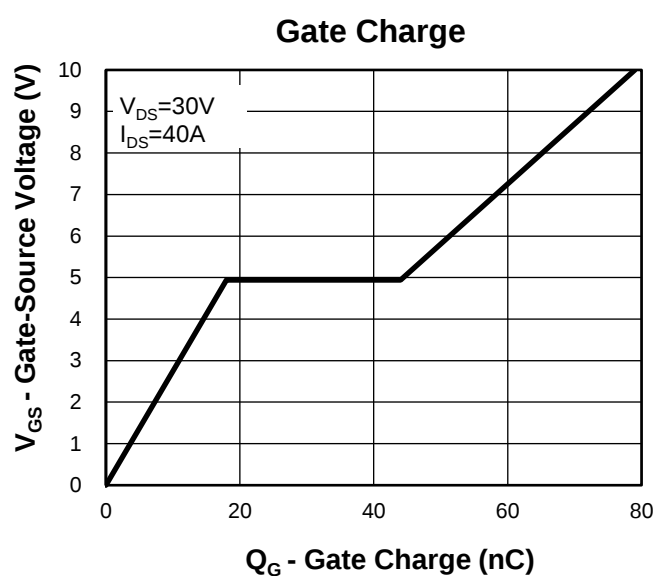
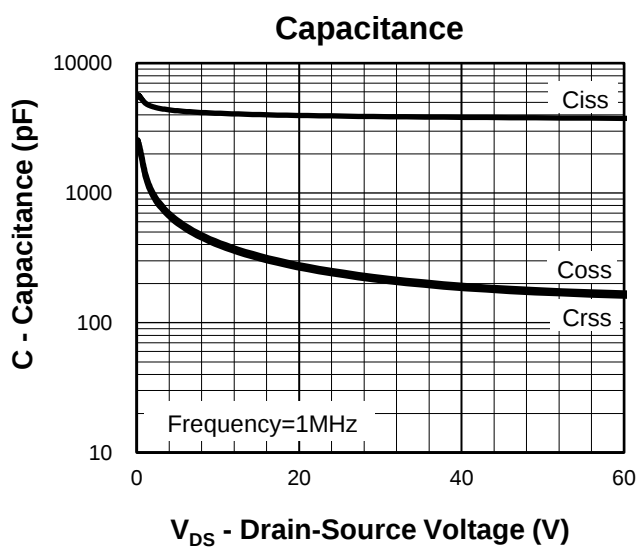
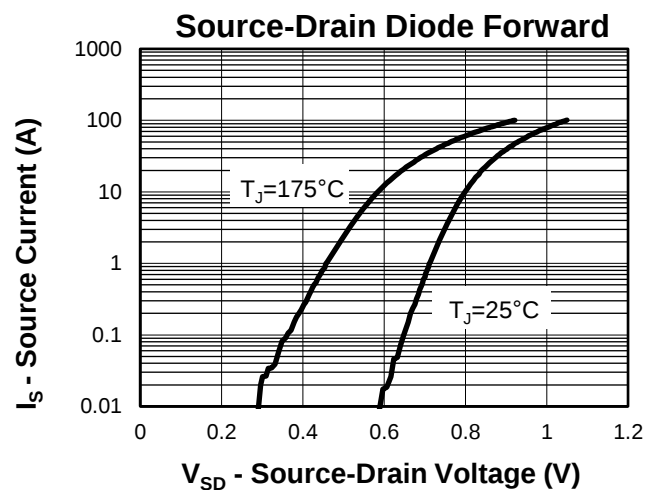
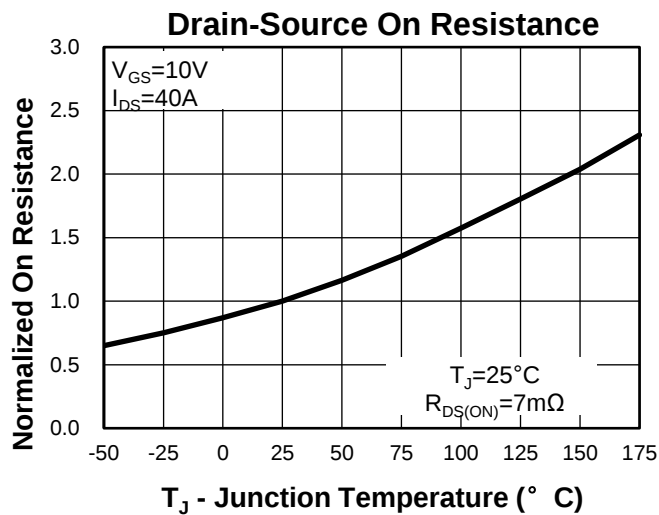
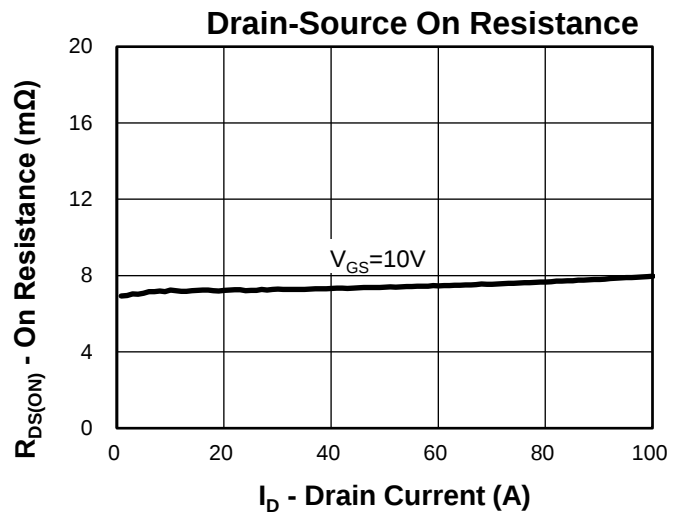
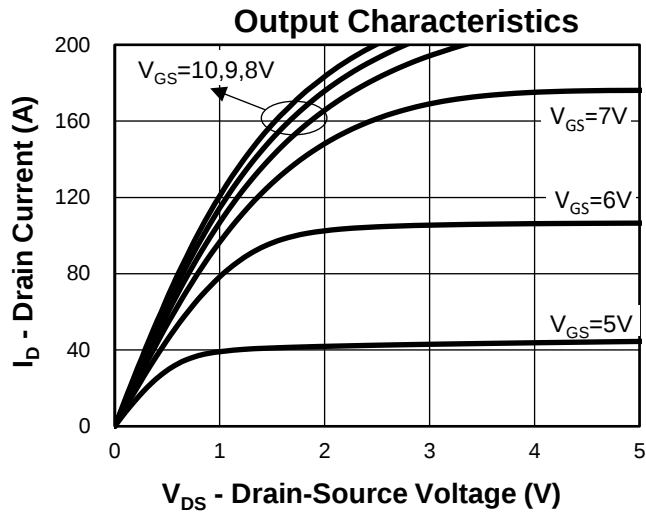
2nd Line: Part Number(6205)

3rd Line: Lot Number(YWWXXX)

Typical Characteristics

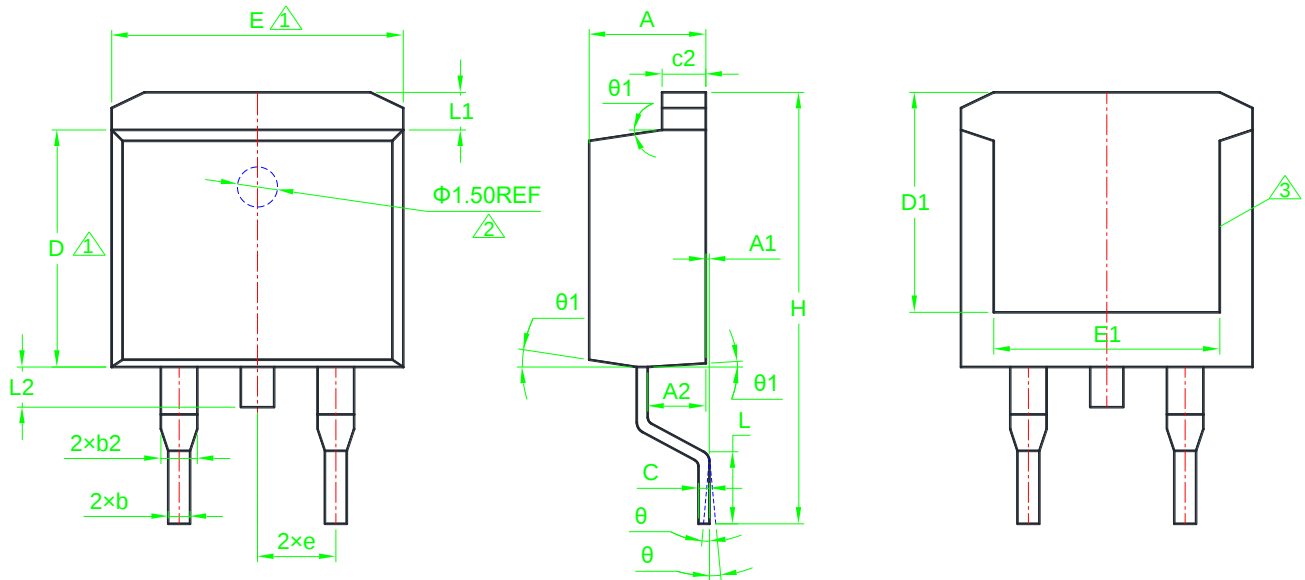


Typical Characteristics



Package Information

TO-263



SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.50	4.80	0.169	0.177	0.189	e	2.54BSC			0.100BSC		
A1	0.00	0.10	0.25	0.000	0.004	0.010	E	9.90	10.10	10.30	0.390	0.398	0.406
A2	2.20	*	2.80	0.087	*	0.110	E1	7.00	*	8.50	0.276	*	0.335
b	0.70	0.85	0.95	0.028	0.033	0.037	H	14.80	*	15.70	0.583	*	0.618
b2	1.15	*	1.47	0.045	*	0.058	L	2.10	*	2.79	0.083	*	0.110
c	0.38	*	0.65	0.015	*	0.026	L1	1.10	*	1.42	0.043	*	0.056
c2	1.20	1.30	1.40	0.047	0.051	0.055	L2	1.00	*	1.70	0.039	*	0.067
D	8.40	8.90	9.40	0.331	0.350	0.370	theta	0°	*	8°	0°	*	8°
D1	7.10	*	8.20	0.280	*	0.323	theta 1	3°	*	9°	3°	*	9°

- △1 Dimensions D and E do not include mold flash protrusions or gate burrs.
- △2 The existence and size of demolding hole are variable depending on mold.
- △3 The size and shape of exposed pad are variable depending on mold.

Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms



Diode Recovery Test Circuit and Waveforms



Gate Charge Test Circuit and Waveform



Customer Service

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