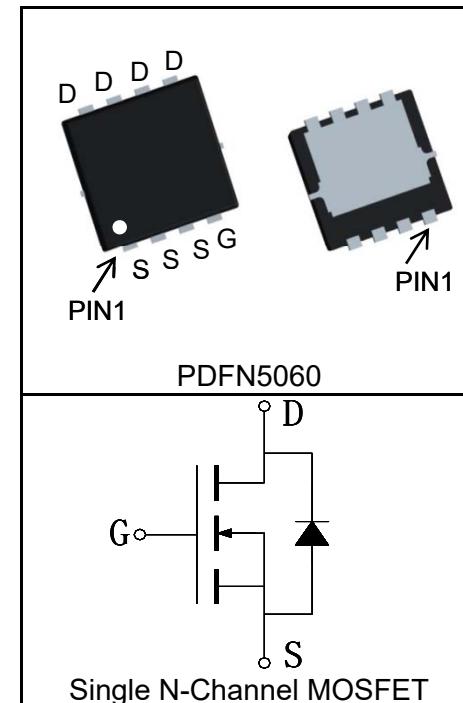


## Features

- 40V/180A,
- $R_{DS\ (ON)} = 2.1\text{m}\Omega$ (Typ.)@ $V_{GS}=10\text{V}$
- Low  $R_{DS\ (ON)}$
- Super High Dense Cell Design
- Fast Switching Speed
- 100% avalanche tested

## Pin Description



## Applications

- Switching Application Systems



Halogen-Free

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
<b>Common Ratings</b> ( $T_C=25^\circ\text{C}$ Unless Otherwise Noted)			
$V_{DSS}$	Drain-Source Voltage	40	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	
$T_J$	Maximum Junction Temperature	150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_S$	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$	180
			A

### Mounted on Large Heat Sink

$I_{DP}^{(1)}$	300 $\mu\text{s}$ Pulse Drain Current Tested	$T_C=25^\circ\text{C}$	720	A
$I_D^{(2)}$	Continuous Drain Current@ $T_C(V_{GS}=10\text{V})$	$T_C=25^\circ\text{C}$	180	A
		$T_C=100^\circ\text{C}$	114	
	Continuous Drain Current@ $T_A(V_{GS}=10\text{V})^{(3)}$	$T_A=25^\circ\text{C}$	30	
		$T_A=70^\circ\text{C}$	24	
$P_D$	Maximum Power Dissipation@ $T_C$	$T_C=25^\circ\text{C}$	125	W
		$T_C=100^\circ\text{C}$	50	
	Maximum Power Dissipation@ $T_A$ <sup>(3)</sup>	$T_A=25^\circ\text{C}$	3.5	
		$T_A=70^\circ\text{C}$	2.3	

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1	°C/W
$R_{\theta JA}^{(3)}$	Thermal Resistance-Junction to Ambient	35	°C/W
<b>Drain-Source Avalanche Ratings</b>			
$E_{AS}^{(4)}$	Avalanche Energy, Single Pulsed	900	mJ

**Electrical Characteristics** ( $T_C=25^\circ C$  Unless Otherwise Noted)

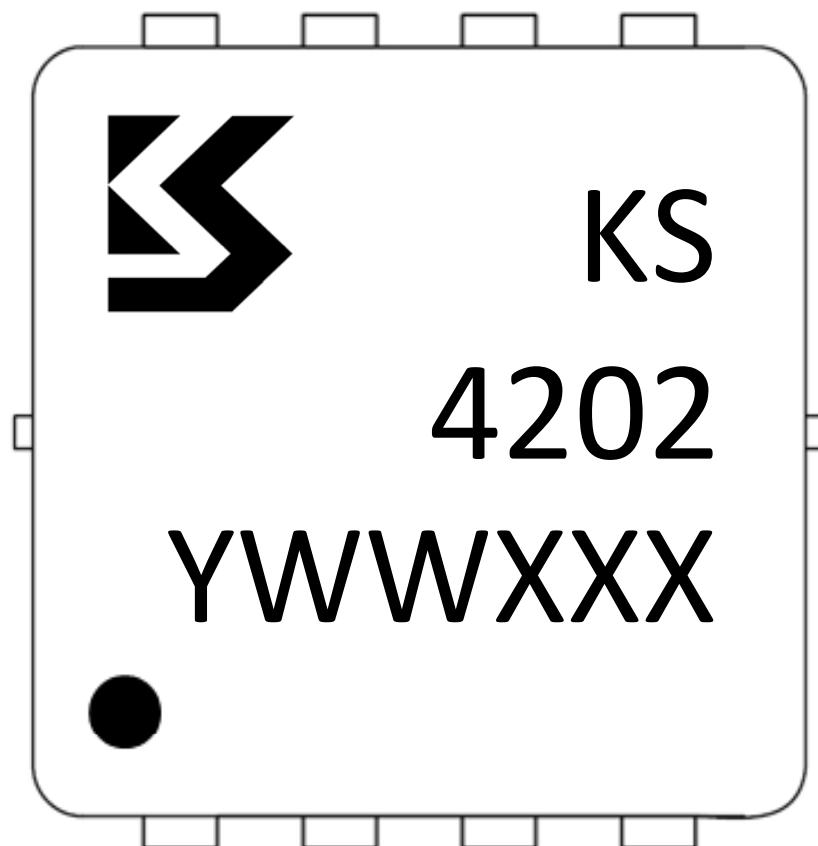
Symbol	Parameter	Test Condition	KS4202NA			Unit
			Min.	Typ.	Max.	
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	40			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$			1	$\mu A$
		$T_J=125^\circ C$			30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	2	3	4	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
$R_{DS(ON)}^{(5)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=20A$		2.1	2.4	$m\Omega$
<b>Diode Characteristics</b>						
$V_{SD}^{(5)}$	Diode Forward Voltage	$I_{SD}=20A, V_{GS}=0V$		0.78	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD}=20A, dI_{SD}/dt=100A/\mu s$		77		ns
$Q_{rr}$	Reverse Recovery Charge			53		nC
<b>Dynamic Characteristics</b> <sup>(6)</sup>						
$R_G$	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$		1.8		$\Omega$
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=20V, Frequency=1.0MHz$		5020		$pF$
$C_{oss}$	Output Capacitance			790		
$C_{rss}$	Reverse Transfer Capacitance			290		
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=20V, I_{DS}=20A, V_{GS}=10V, R_G=3\Omega$		19		ns
$t_r$	Turn-on Rise Time			67		
$t_{d(OFF)}$	Turn-off Delay Time			49		
$t_f$	Turn-off Fall Time			31		
<b>Gate Charge Characteristics</b> <sup>(6)</sup>						
$Q_g$	Total Gate Charge	$V_{DS}=20V, V_{GS}=10V, I_{DS}=20A$		74		nC
$Q_{gs}$	Gate-Source Charge			23		
$Q_{gd}$	Gate-Drain Charge			26		

## Notes:

- ①Pulse width limited by safe operating area.
- ②Calculated continuous current based on maximum allowable junction temperature. The package limitation current is 50A.
- ③When mounted on 1 inch square copper board,  $t \leq 10\text{sec}$ .
- ④Limited by  $T_{J\max}$ ,  $I_{AS} = 60\text{A}$ ,  $L = 0.5\text{mH}$ ,  $V_{DD} = 20\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
- ⑤Pulse test; Pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- ⑥Guaranteed by design, not subject to production testing.

**Ordering and Marking Information**

Device	Package	Packaging	Quantity	Reel Size	Tape width
KS4202NA	PDFN5060	Tape&Reel	5000	13"	12mm

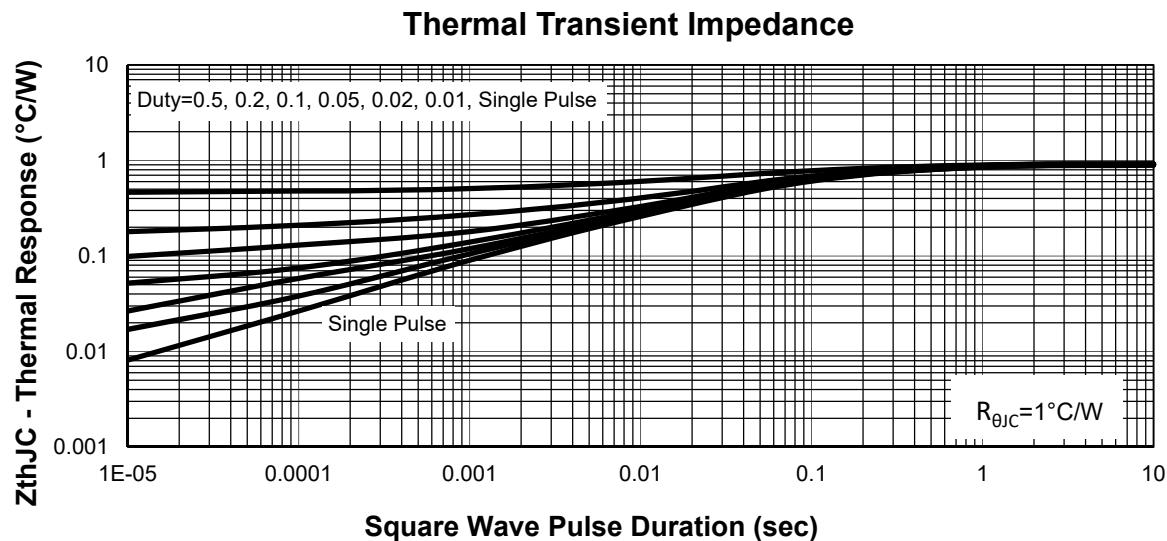
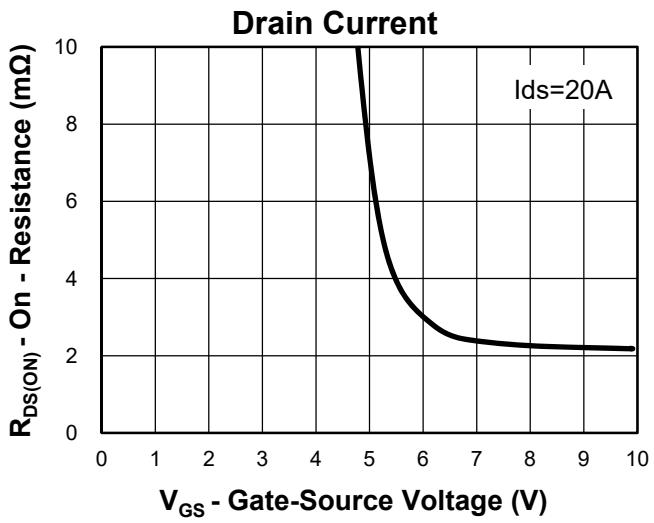
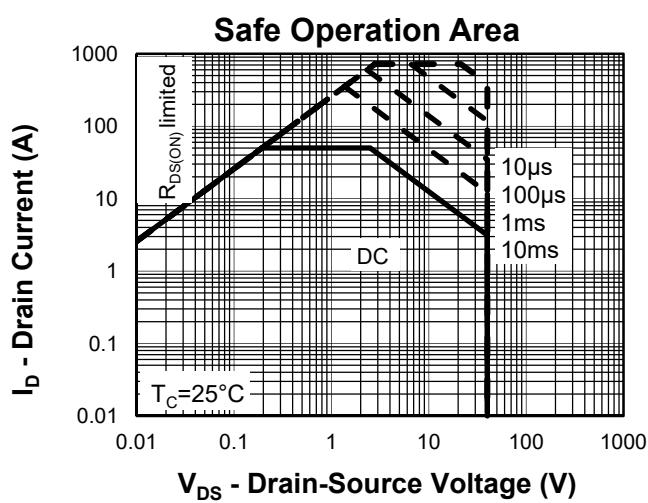
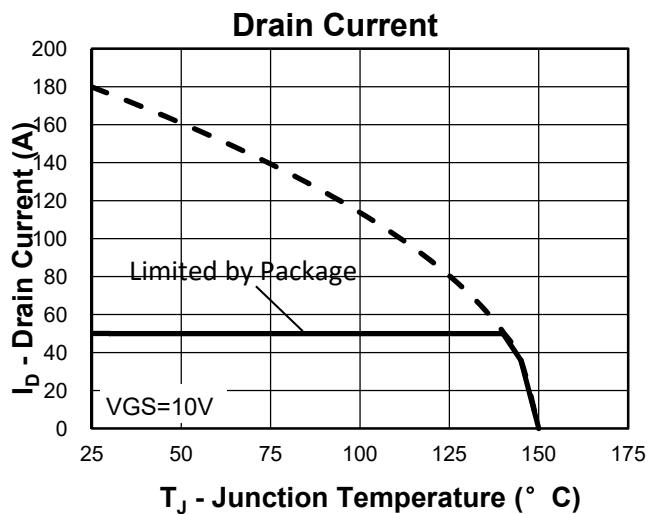
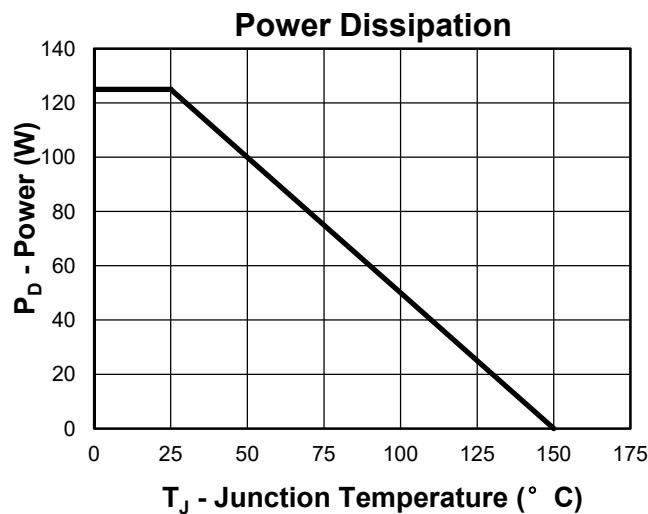


Y = Year, 2017-A, 2018-B, etc.

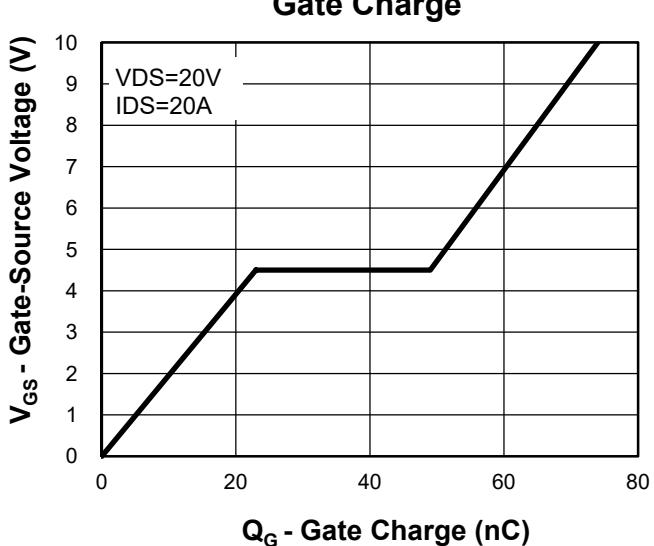
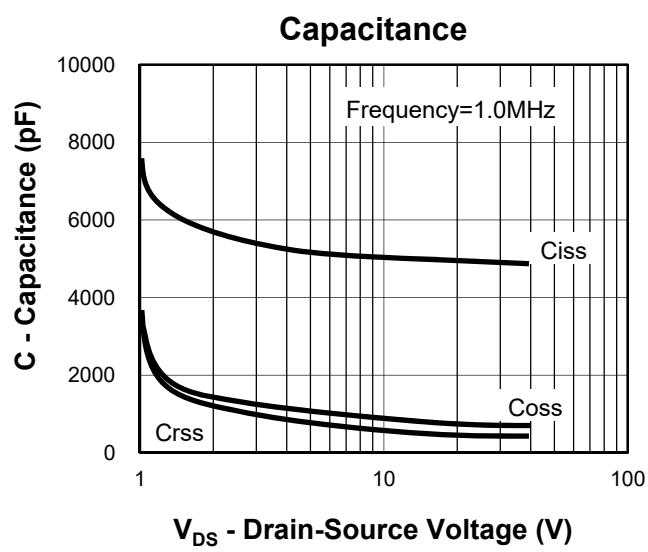
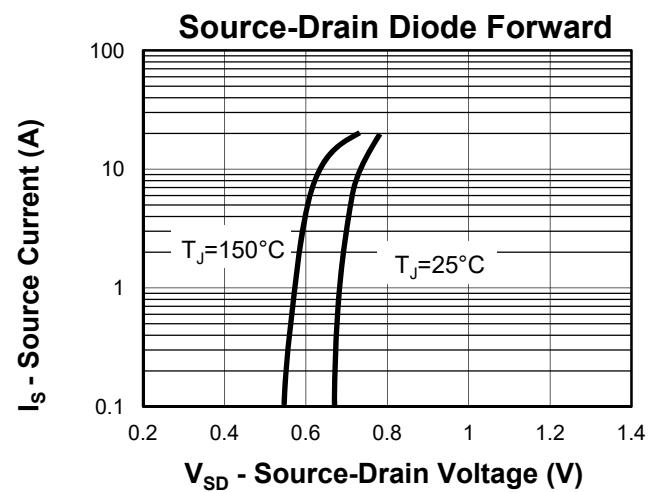
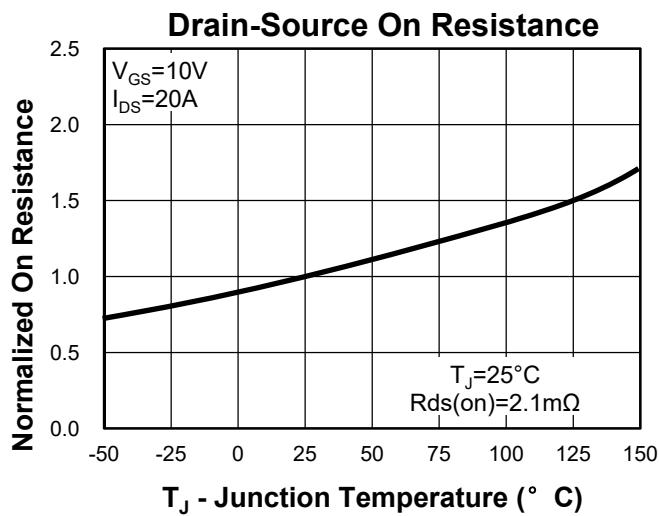
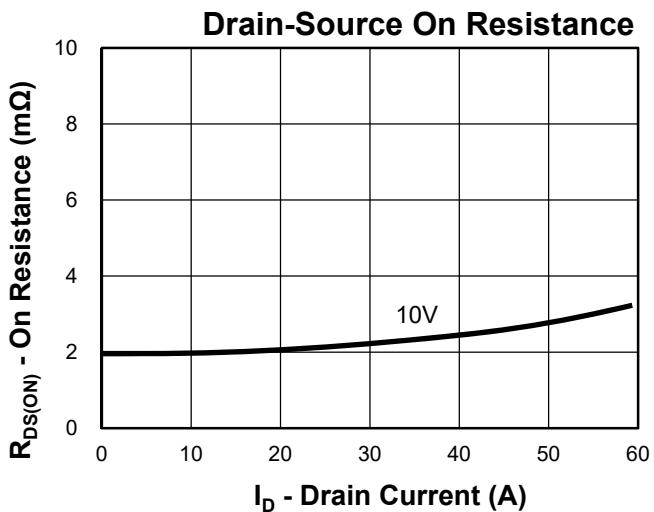
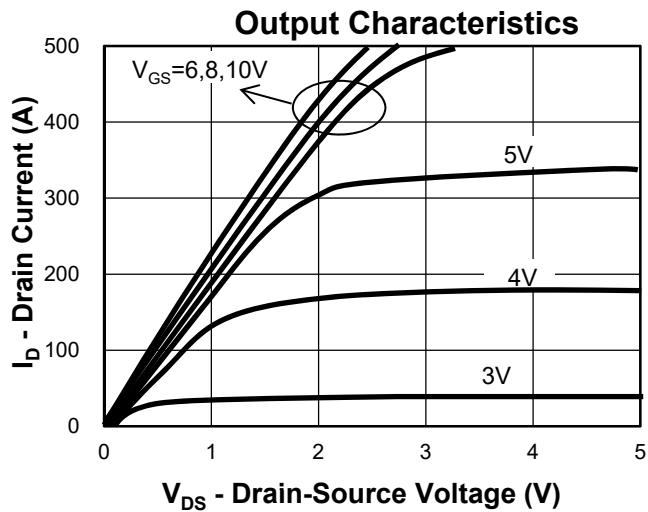
WW = Week.

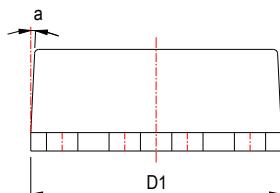
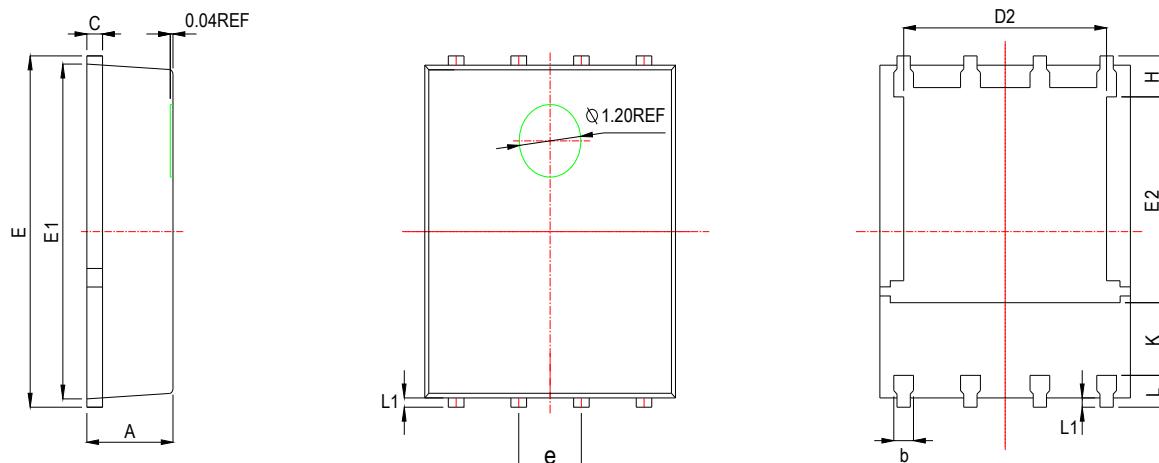
XXX = Lot number.

## Typical Characteristics

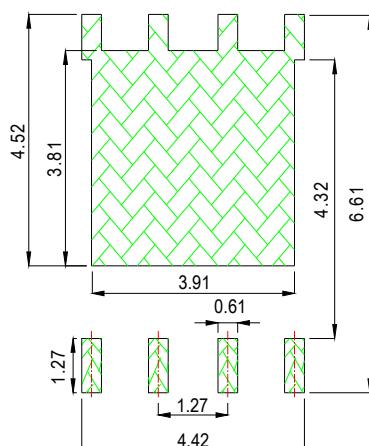


## Typical Characteristics



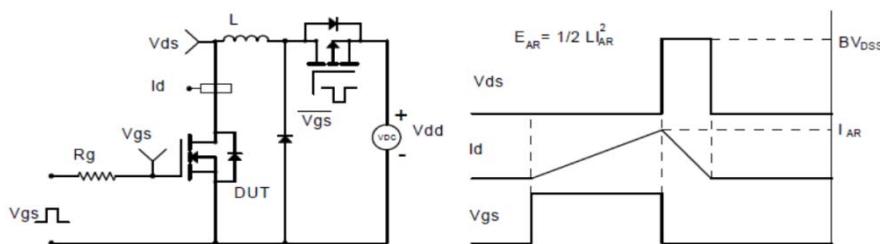
**Package Information**
**PDFN5060**


**Land Pattern**  
(Only for Reference )

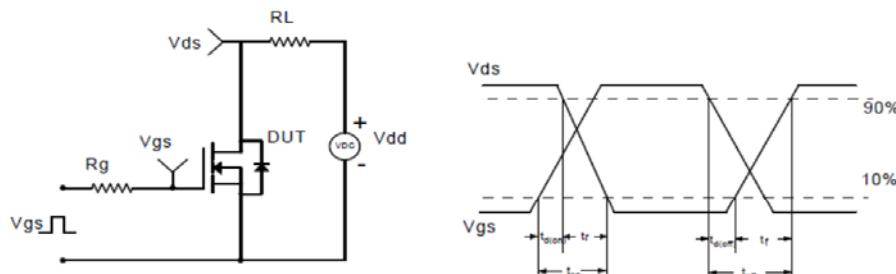


SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
b	0.33	0.42	0.51	0.013	0.017	0.020
c	0.20	0.25	0.30	0.008	0.010	0.012
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.61	3.79	3.96	0.142	0.149	0.156
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	5.65	5.75	5.85	0.222	0.226	0.230
E2	3.38	3.58	3.78	0.133	0.141	0.149
e	1.27 BSC			0.005 BSC		
H	0.41	0.51	0.61	0.016	0.020	0.024
k	1.10			0.043		
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
a	0°		12°	0°		12°

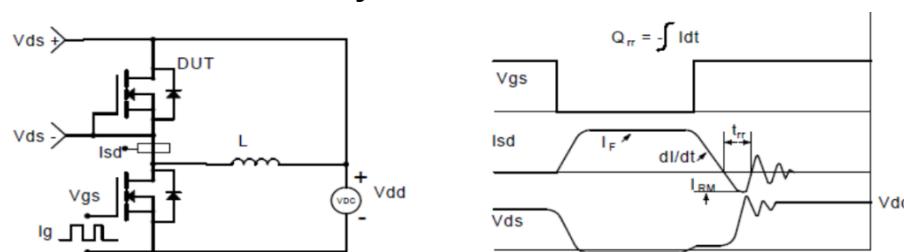
### Avalanche Test Circuit and Waveforms



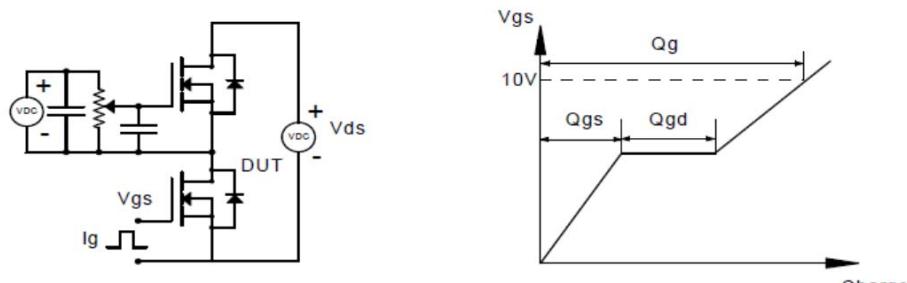
### Switching Time Test Circuit and Waveforms



### Diode Recovery Test Circuit and Waveforms



### Gate Charge Test Circuit and Waveform



### Customer Service

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Web:[www.kwansemi.com](http://www.kwansemi.com)

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