

Features

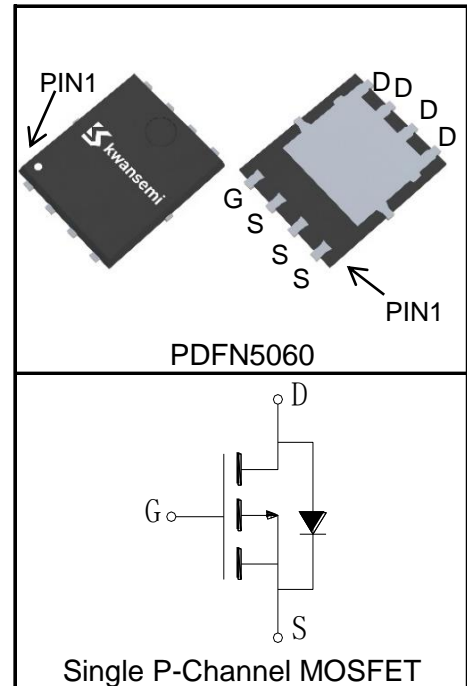
- -20V/-130A,
 $R_{DS(ON)} = 2.2m\Omega(Typ.)@V_{GS}=-4.5V$
 $R_{DS(ON)} = 3.1m\Omega(Typ.)@V_{GS}=-2.5V$
 $R_{DS(ON)} = 5.4m\Omega(Typ.)@V_{GS}=-1.8V$
- Low $R_{DS(ON)}$
- Super High Dense Cell Design
- Fast Switching Speed
- 100% avalanche tested

Applications

- Switching Application Systems



Pin Description



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
Common Ratings ($T_C=25^\circ C$ Unless Otherwise Noted)			
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	± 12	V
T_{Jmax}	Maximum Junction Temperature	150	$^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ C$
I_S	Diode Continuous Forward Current	$T_C=25^\circ C$ -130	A
Mounted on Large Heat Sink			
$I_{DP}^{①}$	Pulse Drain Current	$T_C=25^\circ C$ -520	A
$I_D^{②}$	Continuous Drain Current@ $T_C(V_{GS}=-4.5V)$	$T_C=25^\circ C$	-130
		$T_C=100^\circ C$	-82
	Continuous Drain Current@ $T_A(V_{GS}=-4.5V)^{③}$	$T_A=25^\circ C$	-33
		$T_A=70^\circ C$	-27
P_D	Maximum Power Dissipation@ T_C	$T_C=25^\circ C$	62
		$T_C=100^\circ C$	25
	Maximum Power Dissipation@ $T_A^{③}$	$T_A=25^\circ C$	4.2
		$T_A=70^\circ C$	2.7

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2	°C/W
$R_{\theta JA}$ ^③	Thermal Resistance-Junction to Ambient	30	°C/W
Drain-Source Avalanche Ratings			
E_{AS} ^④	Avalanche Energy, Single Pulsed	361	mJ

Electrical Characteristics ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	KS23042NA			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=-250\mu A$	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V$			-1	μA
		$T_J=125^\circ C$			-30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250\mu A$	-0.4	-0.7	-1	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$			± 100	nA
$R_{DS(ON)}$ ^⑤	Drain-Source On-state Resistance	$V_{GS}=-4.5V, I_{DS}=-20A$		2.2	2.6	m Ω
		$V_{GS}=-2.5V, I_{DS}=-15A$		3.1	3.9	m Ω
		$V_{GS}=-1.8V, I_{DS}=-10A$		5.4	7	m Ω
Diode Characteristics						
V_{SD} ^⑤	Diode Forward Voltage	$I_{SD}=-20A, V_{GS}=0V$		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD}=-20A, dI_{SD}/dt=100A/\mu s$		38		ns
Q_{rr}	Reverse Recovery Charge			106		nC
Dynamic Characteristics ^⑥						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$		3.3		Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=-10V,$ Frequency=200KHz		10250		pF
C_{oss}	Output Capacitance			1475		
C_{rss}	Reverse Transfer Capacitance			1330		
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-10V, I_{DS}=-20A,$ $V_{GS}=-4.5V, R_G=3\Omega$		49		ns
t_r	Turn-on Rise Time			88		
$t_{d(OFF)}$	Turn-off Delay Time			101		
t_f	Turn-off Fall Time			67		
Gate Charge Characteristics ^⑥						
Q_g	Total Gate Charge	$V_{DS}=-10V, V_{GS}=-4.5V,$ $I_{DS}=-20A$		53		nC
Q_{gs}	Gate-Source Charge			12		
Q_{gd}	Gate-Drain Charge			14		

Notes:

- ①Pulse width limited by safe operating area.
- ②Calculated continuous current based on maximum allowable junction temperature. The package limitation current is 50A.
- ③When mounted on 1 inch square copper board, $t \leq 10\text{sec}$.
- ④Limited by $T_{J\text{max}}$, Starting $T_J = 25^\circ\text{C}$, $I_{AS\text{max}} = -38\text{A}$, $L=0.5\text{mH}$, $V_{DD} = -30\text{V}$, $R_G = 25\Omega$, $V_{GS} = -4.5\text{V}$. Part not recommended for use above this value. 100% Final Test at $I_{AS} = -21\text{A}$, $L=0.5\text{mH}$.
- ⑤Pulse test; Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- ⑥Guaranteed by design, not subject to production testing.

Ordering and Marking Information

Device	Package	Packaging	Quantity	Reel Size	Tape width
KS23042NA	PDFN5060	Tape&Reel	5000	13"	12mm

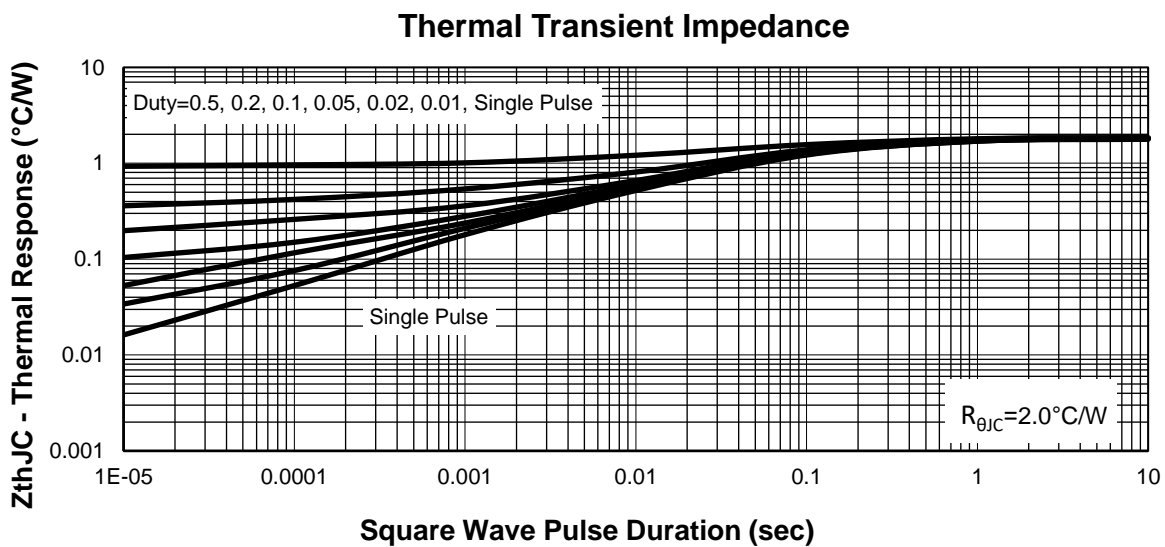
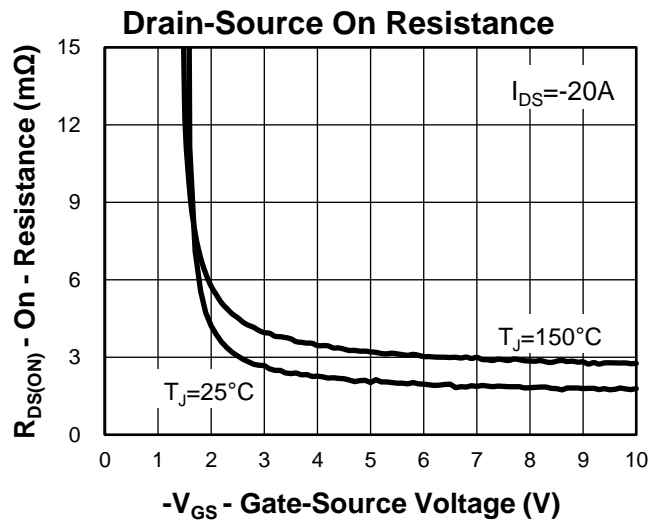
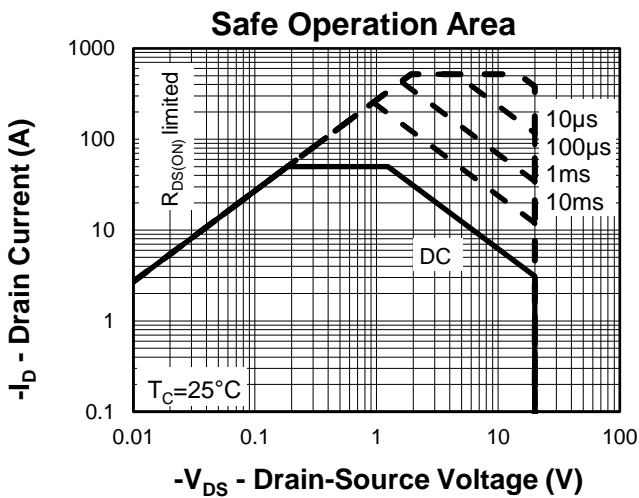
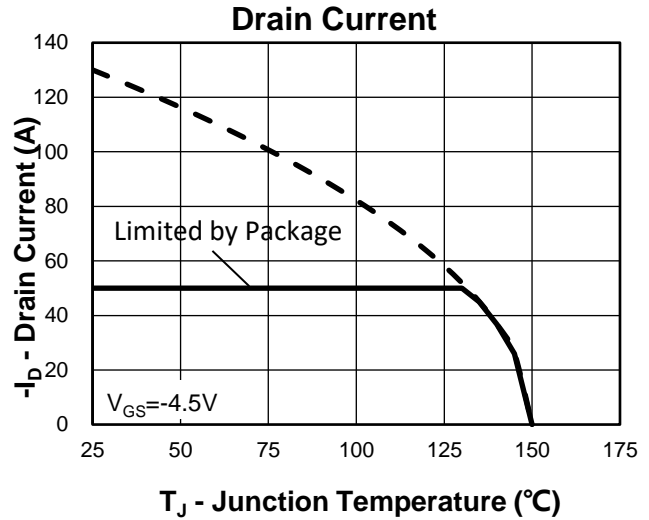
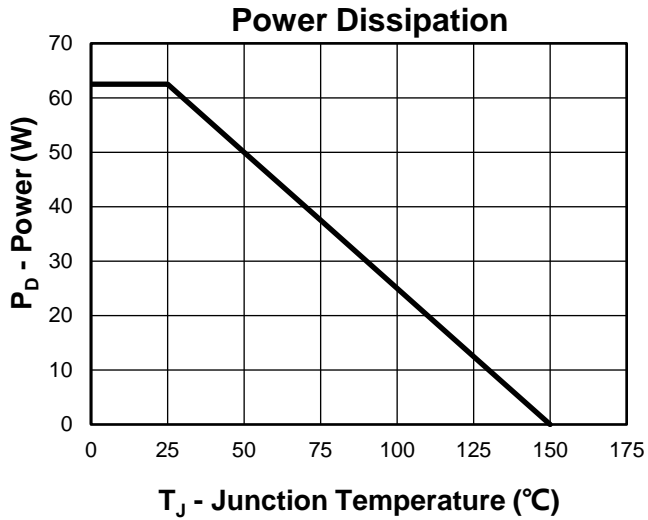


1st Line: Kwansemi LOGO, Kwansemi Code(KS)

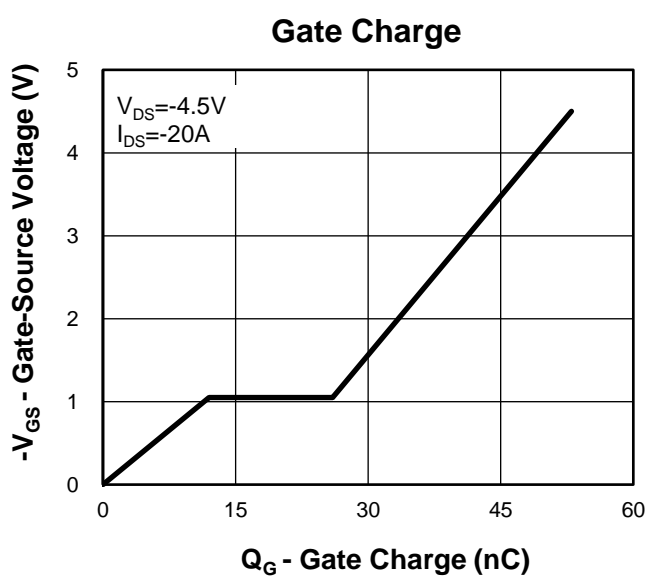
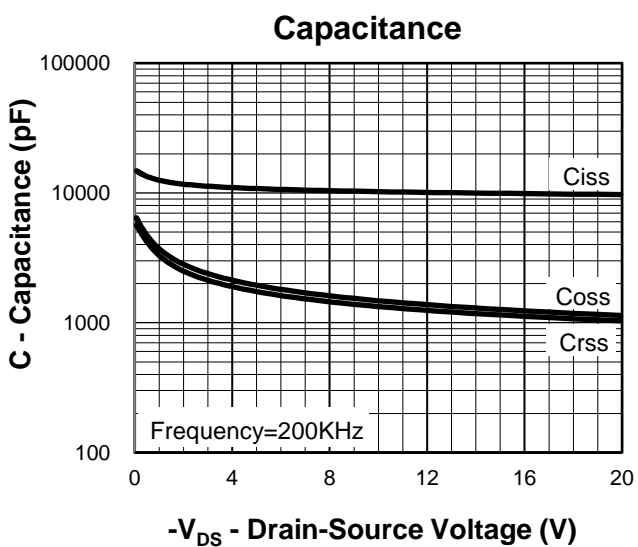
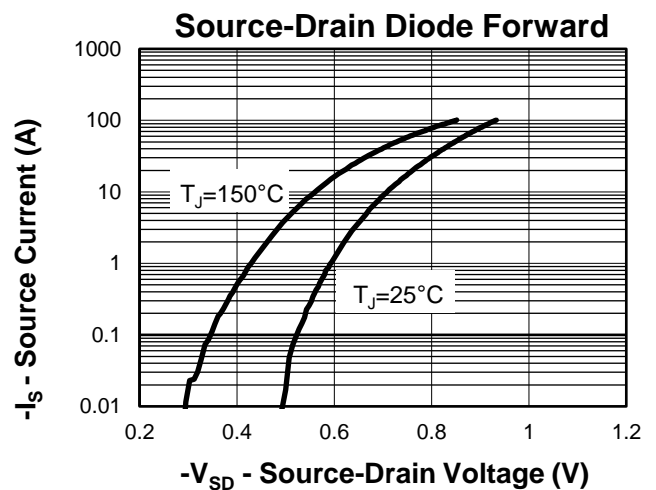
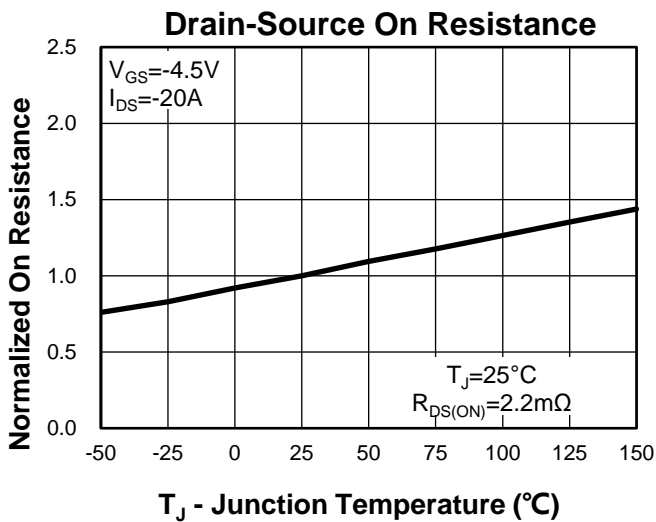
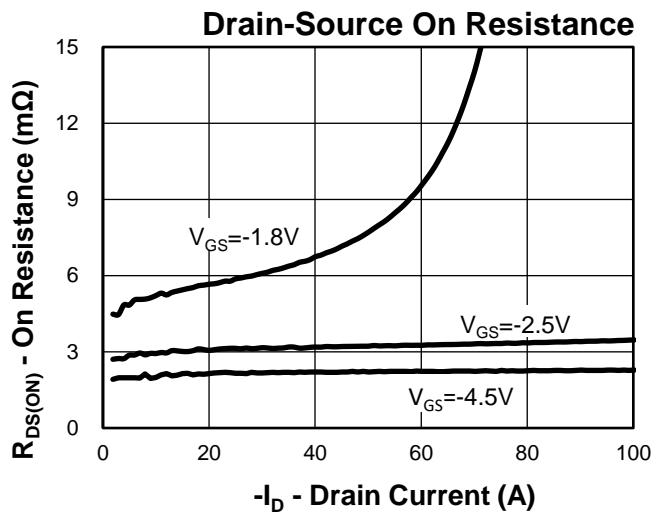
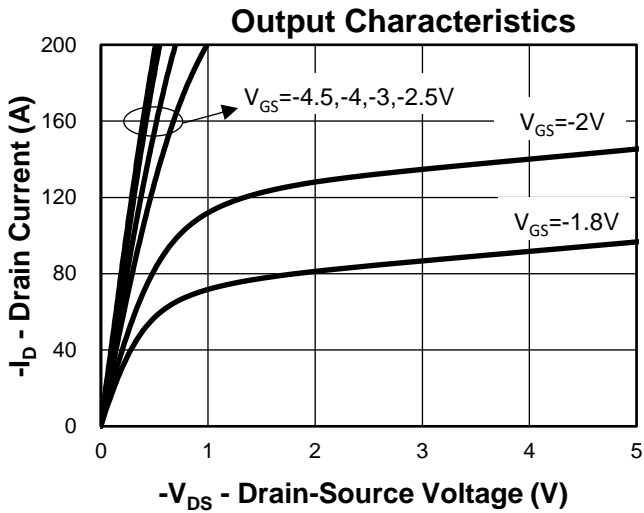
2nd Line: Part Number(23042)

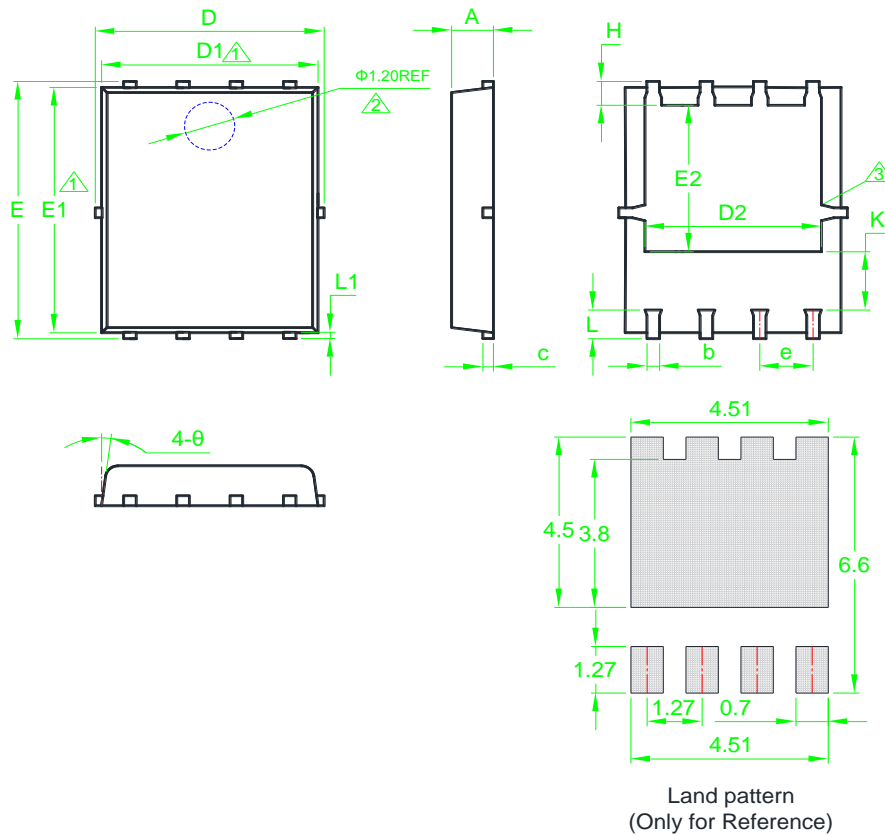
3rd Line: Lot Number(YWWXXX)

Typical Characteristics



Typical Characteristics



Package Information
PDFN5060


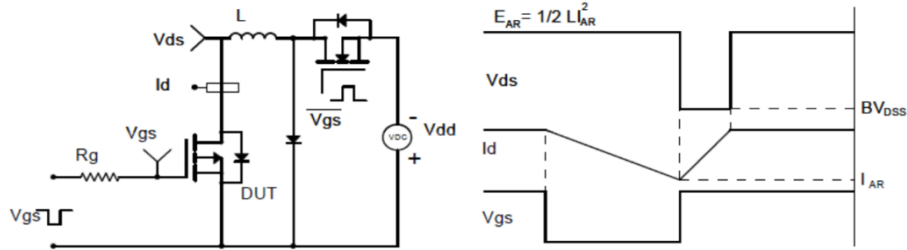
SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.20	0.035	0.039	0.047	E2	3.27	3.50	3.90	0.129	0.138	0.154
b	0.25	*	0.50	0.010	*	0.020	e	1.27BSC			0.050BSC		
c	0.20	0.25	0.30	0.008	0.010	0.012	H	0.41	0.51	0.71	0.016	0.020	0.028
D	5.15BSC			0.203BSC			K	1.10	1.35	1.50	0.043	0.053	0.059
D1	4.80	5.00	5.40	0.189	0.197	0.213	L	0.51	0.61	0.71	0.020	0.024	0.028
D2	3.60	*	4.40	0.142	*	0.173	L1	0.06	0.13	0.30	0.002	0.005	0.012
E	5.90	6.15	6.30	0.232	0.242	0.248	θ	0°	*	12°	0°	*	12°
E1	5.40	5.80	5.95	0.213	0.228	0.234							

① Dimensions D1 and E1 do not include mold flash protrusions or gate burrs.

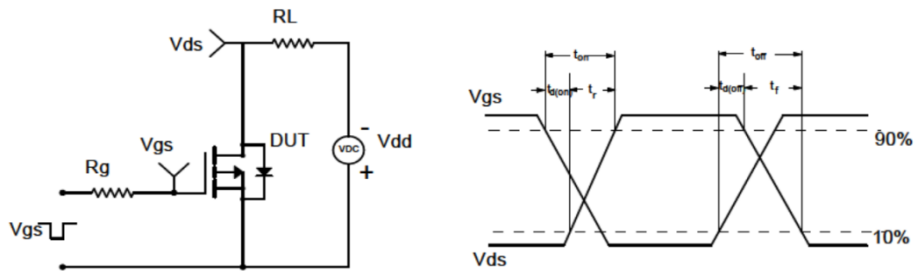
② The existence and size of demolding hole are variable depending on mold.

③ The size and shape of exposed pad are variable depending on mold.

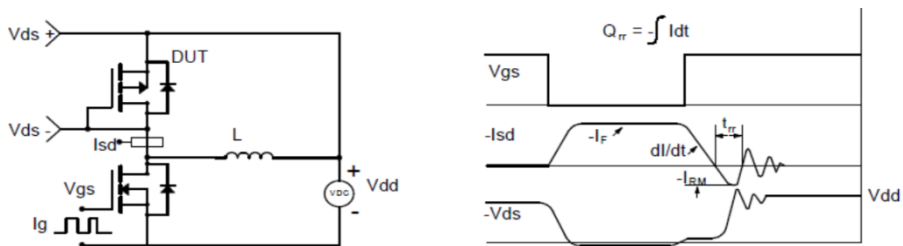
Avalanche Test Circuit and Waveforms



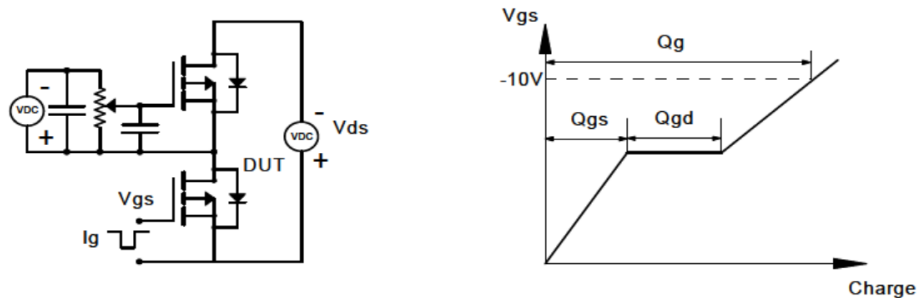
Switching Time Test Circuit and Waveforms



Diode Recovery Test Circuit and Waveforms



Gate Charge Test Circuit and Waveform



Customer Service

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